IBA TECHNICAL REVIEW

3

Digital Television

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Introduction

Since the earliest days of Baird and Blumlein, television signals have been a curious mixture of analogue and pulse techniques – a combination that has given good service in its time but which represents at the best an uneasy alliance, at the worst an inelegant and fragile hybrid. The transmission engineer, the recording engineer – indeed virtually all those concerned with processing or handling colour television signals – must welcome the prospect of a more rugged, more mathematical signal. And this is what is offered by digital techniques: signals in which all waveforms are drawn from just a selected few; signals which are neither level dependent nor phase dependent; in which the errors follow calculable rules; signals which can be readily regenerated no matter how many generations away from the original.

A television waveform based on digital techniques can offer all the certainty and accuracy of an arithmetical calculation, but still offers the challenge that one needs to think in terms of a hundred million binary digits a second; speeds at which even the mobile electron and the highest speed logic seem relatively slow.

Yet notable advances have already been made by television engineers toward the digital millenium; already it is possible to be sure of the validity of the concept of video signal handling as a purely numerical process, and to advance with confidence towards equipment which will behave precisely in accordance with its design calculations, rather than depend on the skill used in lining-up a whole series of complex analogue circuits. The signs are that television engineering, computer engineering, and communications engineering will, before very long, become more and more closely linked together through the common adoption of digital techniques.

The United Kingdom has already contributed much to these evolutionary changes: the early work by Babbage and others that paved the way to the digital computer; the invention in the mid-thirties of pulse code modulation by Alec Reeves; the recent work by the BBC and industry on the various distribution techniques that have stemmed from 'sound-in-syncs'; and most recently of all the development within the laboratories of the IBA of an experimental – but already operationally proven – field-rate digital standards converter, now in regular service with ITN.

Soon will come other digital techniques – such systems as 'Oracle', for example, open up the possibility of important new uses of the television receivers in our homes (*see page* 61); digital video recording cannot be long delayed; the transmission of vast amounts of digitalized information along wide-band light pipes is no longer just a remote possibility. And behind the gradual acceptance of digital techniques for specialized applications in television broadcasting lies the exciting possibility of an all-digital system – at least, that is, until the signals actually reach the transmitters. Such changes will not come overnight; they may never come if there were to be a sudden reversal in the trend toward lower and lower cost handling of bits and cheaper methods of converting from analogue to digital signals and vice versa. But all the signs are that in the economic battle the victory will go to the digits, and that studio complexes based almost entirely on digital signals will be first as economic and then more economic than the present fickle combination of analogue and pulse waveforms.

This volume of the *IBA Technical Review* is devoted to digital television. It has two main purposes: to provide a working introduction to digital techniques for those television engineers who are more used to the traditional approach; and to report a little of what has already been achieved in a number of specific projects. Many of these projects are still continuing and may well extend in scope.

by F Howard Steele,
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An Introduction to Integrated Circuits and Digital Electronics

by Pat Hawker

Synopsis

In recent years the broadcast engineer has witnessed the very rapid spread of integrated-circuit techniques and is now increasingly faced with the need to understand a whole new world of digital terms and techniques. This introductory section is intended for those still struggling to understand these new systems; to set the scene; to concentrate on the basics; to explain at least something of the jargon and terminology of the new electronics.

Those fortunate engineers who have already worked with the devices and techniques of digital electronics can safely skip this section and go straight to the heady world of the practical applications – for the others it is hoped that these brief notes will provide a background to the later sections.

INTEGRATED CIRCUITS

Integrated circuits (abbreviated IC) represent complete electronic circuits packaged into a compact unit, usually including both active devices (transistors, MOSFETS, diodes) and passive components (resistors and capacitors), with the necessary interconnections (sometimes called intraconnections to distinguish them from connections made outside the module) and the numbers of lead-out wires to allow the device to be used with other modules or discrete components. An integrated circuit is thus a complete circuit building block.

The most common form is the semiconductor integrated circuit (SIC) in its monolithic form in which the entire circuit block is formed within a single piece of semiconductor material (usually silicon) by a succession of diffusion processes within one tiny wafer (also called SLICE, DIE, or DICE). A monolithic SIC is sometimes referred to as a solid circuit; alternative forms are mostly of hybrid form using combinations of fabrication techniques.

The SIC is generally a mass-produced device based on standard electronic circuits, but hybrid, multichip, thin-film and thick-film ICS are often made in small quantities for specified applications.

In the chip or multichip form, the components are fabricated on separate pieces of semiconductor material and then assembled into the complete package. Thin-film integrated circuits have connections, resistors and capacitors deposited on extremely thin films on insulating substrates (e.g. glass) usually with the active devices added afterwards; active devices made for this purpose are usually not initially fully encapsulated and are termed flip-chip devices.

Thick-film integrated circuits are basically similar to thin-film units except that the film is significantly 'thicker' (but still usually only about one-thousandth of an inch thick).

The main forms of IC are often known by the style of their packaging and encapsulation; in the top-hat or TO5 transistor metal can, or in the lowest-cost bead-like epoxy units, with the lead-out wires spaced around the circumference; as compact rectangular flat-box units, termed flat-packs, with the connecting wires coming out of the sides; or as the dual in-line, basically akin to flat-packs but with the emerging wires or strips turned through 90° to ease assembly in printed-circuit boards or insertion into sockets.

Most of the early integrated circuits were based on planar bipolar transistors as the active devices. Modern units often have active devices of field effect or metal-oxide-semiconductors form; these may then be termed MOSICs or (since MOS is one form of metal-insulated-semiconductor) MISICs. A special form of MOSIC uses complementary-symmetry MOS devices in what are called COSMOS or COS/MOS or CMOS; the use of combinations of large numbers of n-channel and p-channel MOSFETs allows quite complex logic circuits to be realized without using any passive components such as resistors or capacitors.

Initially most monolithic ICs were designed for digital or logic applications in which signals are essentially only of 'go or no-go' form. However, many devices for communications applications are suitable for handling conventional complex analogue waveforms – these are often termed linear integrated circuits (LIC).

Many linear ICs are purpose-designed for specific types of applications; however, a widely-used category of general-purpose LIC is the operational amplifier. This term originally came into general use to define types of discrete-component amplifiers designed to perform the mathematical operations in analogue computers. In these computers different functions were achieved with a basic building-block type of amplifier by varying the feedback networks; to allow this to happen, the amplifiers featured high-voltage gain, high input impedance, low drift, and good stability under various feedback conditions, together with low output impedance and low noise factor. When operational amplifiers became available in integrated-circuit form, they became attractive for many different purposes, and can be regarded as a packaged linear amplifier which can be made to have a wide range of gain by varying the degrees of feedback.

Another category of linear units are the microwave integrated circuits (MIC) in which special techniques are incorporated to make them suitable for use at microwave frequencies and to facilitate their incorporation in equipments featuring microstrip, slab-line and strip-line forms of construction.

Generally, during manufacture of standard monolithic integrated circuits, large numbers of similar circuit blocks are fabricated on a master slice (about 1 in. in diameter) and then cut into large numbers of individual tiny circuit modules by scribing. This makes it possible instead to manufacture integrated circuits having many thousands of component functions by utilizing possibly the whole of a master slice; however, this means that every component must be perfectly formed so that the yield (percentage of good devices to total manufactured) is much lower than when large numbers of small circuits are made from a master slice and can then be sorted into good or defective units. Where very large circuits are made in one package, this is termed large scale integration (LSI); while for units roughly between normal SIC complexity and LSI, devices are termed medium scale integration (MSI).

Advantages of integrated circuits

Compared with discrete components, the use of integrated circuits makes possible the construction of complex circuits with little more constructional complexity than would be involved in a single stage when using discrete components; they also make possible equipments of smaller size and lower weight, or block amplifiers of very high gain with low-phase shifts. Many standard integrated circuits are available at a cost per function significantly lower than for the equivalent discrete components.

Disadvantages of integrated circuits

The integrated circuit may introduce unwanted parasitic coupling between its various components, including the formation of parasitic transistors and diodes; only a limited range of resistor and capacitor values can be economically provided; there is usually low precision in resistor values; high temperature coefficients may be involved (usually making the IC unsuitable for stable oscillator applications); it is virtually impossible to make inductors an integral part of the IC unless 'active filter' (gyrator) techniques are used; there may be a problem in dissipating heat in the tiny volume; and the cost of specialized units may be high (some devices cost in the region of £10).

The SIC, it should be noted, is not a 'module' containing a large number of components which could be connected in different ways, but is a complete circuit having a finite number of leads brought out (up to about 22), so that there is a limited number of uses to which any particular device can be put. It is clearly an advantage to have these in the form of basic repetitive circuits, of which very large numbers may be used in computors and data processing equipment; in addition there are now units intended specifically for linear circuits as used in television receivers.

Since the circuit is pre-formed, at one time it was suggested that the coming of SICs would virtually eliminate the work of circuit designers, but in practice it is becoming clear that there is still plenty of scope for devising ways in which these units can be put together, or combined with external components to form efficient and novel circuits. And because there are serious limitations, at present, to the component values in SIC circuits, it results in a different approach to circuits in general.

For instance, a high value resistor or large capacitance capacitor takes up far more of the basic silicon slice area than does a transistor; so that it may be preferable to use a whole string of transistors just to get rid of the need for a single resistor or capacitor (it has been said, for example, that it is worth using five transistors to eliminate a single 47 kΩ resistor, and capacitors impose an even heavier penalty in slice area). A transistor takes up about one-third of the slice area required for a 10 pF capacitor, and one-half that of 1 000 Ω ohm resistor.

In most monolithic silicon SICs there is a limit of roughly 20 kΩ to resistor values and 200 pF to capacitors, but many units are designed for lower values than these. A considerably wider range of values is possible with thin film and multichip devices, but even here there are constraints which must be observed.

At present there is no fully developed way of producing an inductor within an SIC, and this means that any inductors have to be added in the external circuit, if they cannot be eliminated by ingenious circuit design. There is for example the possibility of active filters using capacitors to provide inductance but a more common system to eliminate interstage inductive coupling with various forms of dc-coupled amplifiers. The use of dc-coupled amplifiers in IF strips has been exploited in a number of radio and television designs.

DIGITAL ELECTRONICS

A *digital* system is one in which the waveforms are selected from only a restricted number, as opposed to *analogue* systems in which the waveforms may have an infinite number of shapes and amplitudes. The commonly used *binary* system is in fact, a digital system having only two different states, which may be represented by 'go/no-go' codes, including on-off, mark-space, one/zero codes. For example, the Morse code is a binary digital code since it requires for successful transmission only that the receiver can distinguish between the presence or absence of the signal.

Commonly, '1' and '0' states are used: such systems have many advantages in electronics, since they allow the use of standard switching-type and essentially non-critical circuits. A binary digit (e.g. a 0 or a 1) is often called a *bit*. The waveforms of a binary system are essentially pulses, controlled by switches in the form of *logic gates*. The 1 may be of positive or negative polarity with respect to the 0.

In speech and television communication, the basic transducers provide electrical signals of complex analogue waveforms. Increasingly, it is becoming worthwhile to convert these waveforms into digital form for processing and transmission. This can be done by making use of basic *sampling theory* which indicates that if any signal is sampled instantaneously at a rate even slightly higher than twice the highest signal frequency, then the samples will provide all the significant information contained in the original. For example, if a speech signal (say 300–3 500 Hz) is sampled 8 000 times a second, and each of these samples coded in digital form, then we can transmit and handle the speech as though it were extremely high-speed telegraphy, although it will occupy a large bandwidth; systems of this type form the basis of *pulse-code modulation* (PCM) techniques.

It was the development of the electronic computer that underlined the advantages of limiting the number of states and waveforms, and many of the terms used in digital electronics stem from computers and Boolean algebra.

The binary 0, 1 system can utilize the advantages of simple on-off switching and *gating* processes in which a simple signal can control or initiate complex operations. Gates utilize the switching characteristics of diodes and transistors, and are increasingly being implemented in the form of integrated circuits in a number of 'digital families' (see later). Although digital electronics uses only a limited number of basic circuits, these are often employed in very large numbers; this block-like or building module approach is reflected in the use of *logic diagrams* rather than conventional circuit diagrams.

A *logic* circuit is one that can recognize changes in its input conditions. For example an AND gate provides an output only when signals are applied

simultaneously to its various inputs; an OR gate provides an output if a signal is applied to any of its inputs. The number of inputs a logic element will accept is its *fan in*; the number of subsequent circuits it will control is its *fan out*. Standard logic gates do not have sufficient power capability to actuate display and other output devices directly; for this purpose high-power gates, called *drivers*, are used.

The basic circuit blocks of digital electronics include: gates, inverters, bistables (flip-flop with single stable state). In practice, it is usual to refer to both monostable and bistable circuits as flip-flops. An *inverter* is a circuit which changes the state of the signal (e.g. from 1 to 0 and vice versa); it thus resembles a stage providing a 180° phase change in analogue systems. In addition there are major sub-systems using these basic circuit blocks; counters, shift registers, adders, and accumulators.

A NAND gate is a combination of an AND gate followed by an inverter; a NOR gate combines an OR gate with an inverter. In practice a complete digital system can be formed from NAND or NOR gates (but not both) and flip-flops.

It is often convenient to list all possible combinations of the input and output stages of a logic gate in a truth table: a simple form of a *truth table* for AND, OR, NAND, and NOR gates would be:

Input A	*Input B*	AND *output*	OR *output*	NAND *output*	NOR *output*
0	0	0	0	1	1
0	1	0	1	1	0
1	0	0	1	1	0
1	1	1	1	0	0

Common circuit abbreviations used in digital electronics include: FF flip-flop; FL flip-flop latch; SS single shot; ST Schmitt trigger; HA half-adder; FA full adder.

Since a bistable flip-flop can be considered as a unit with a square loop hysteresis curve (as with ferrite cores) it can provide *memory*. The classic Eccles-Jordan bistable circuit can be formed from a NAND or NOR gate by the cross-coupling of output and input connections. To overcome various limitations in conventional bistable operations, more flexible all-purpose circuits have been evolved; these are often known as the J–K flip-flop; or the RST flip-flop; or the type D flip-flop.

A primary source of timing signals in digital systems is a *clock*; this is comparable to an oscillator in analogue systems but with the output in the form of square-wave pulses. A clock may be variable or crystal-controlled. A digital system controlled by a clock is often termed *synchronous*.

A basic timing element is a monostable multivibrator known as a *delay one-shot*; these may be used in generating delayed pulses or signals of arbitrary width.

An *exclusive*-OR gate is one in which the output assumes the 1 state if one and only one input assumes the 1 state.

A *decoder* is often required between a digital system and the associated display: for example a BCD-*to-decimal decoder* provides ten separate outputs (for 0–9) from binary-coded decimal or four-bit binary data applied to its four input lines (e.g. SN7441AN decoder/driver) in order to allow information to be displayed as figures on, for example, a Nixie tube display.

A *shift-register* is a number of bistable units connected so that whenever a shift pulse is applied to all of its stages, the state (i.e. 0 or 1) is immediately transferred to the next stage and so on. For example, a register might be in the condition 01101011; then a *shift right* would make the register become ?0110101 with the new level in the first bistable and a 1 lost from the final stage. A *left-shift* would result in 10101111? in the register. A shift-register is thus a form of memory in which a number of bits of information can be stored temporarily. If the bit 'pushed out' from one side of a register is fed back to its input, it becomes a *ring counter*; if required the state of the ring counter can be displayed by a series of lamp bulbs, lit for 1 and off for 0, etc.

Combinations of J–K flip-flops can be used to form many types of counters and shift registers by re-arranging the interconnections between them.

A *decade counter* counts directly in the decimal system; a commonly used IC for this is the SN 7490N comprising three J–K flip-flops and one R–S flip-flop.

A *schmitt-trigger* is used as a two-state regenerative circuit in which the output level is determined by the input level.

An *expander* is a device used to increase the fan-in capability of another device.

A *buffer* is used to solve loading problems, consisting for example of an emitter-follower; frequently built into the package of an IC logic gate.

THE LOGIC FAMILIES

Certain families of logic arrangements have come into widespread use, designated by initials such as DTL, RTL, TTL, COS/MOS, etc. While in most cases it is possible to mix these devices, this can result in interfacing problems and the tendency is to use a single family throughout a system. The families differ in the basic gate element; maximum speed of operation (usually specified in MHz representing maximum flip-flop toggling frequency); voltage swing (that is logic levels specified for 1 also called High (H), and 0 or Low (L) potentials); immunity to 'noise' (the *noise margin* is the voltage by which the gate input can vary without causing a change in output, and thus represents the amount of spurious interference at the input that will not appear at – or affect – the output); and power capability (typically specified in milliwatts per gate). In practice, the different IC logic families also tend to be operated from different supply voltage rails. The speed at which a device works hinges upon the *propagation delay*, the time required for a discrete logic level to pass through a single logic stage.

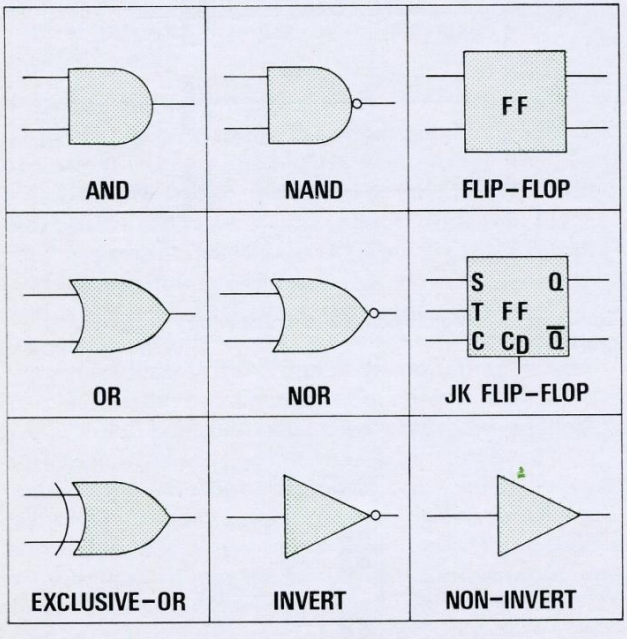


Fig.1. Commonly used symbols in electronic logic circuits.

DTL (diode-transistor-logic)

This is a medium-speed logic family which at first required both positive and negative power sources, but more recently is often suitable for use with a single 5 V line. It can be used fairly readily with TTL logic and also integrates well with discrete components. The voltage thresholds are affected significantly by temperature.

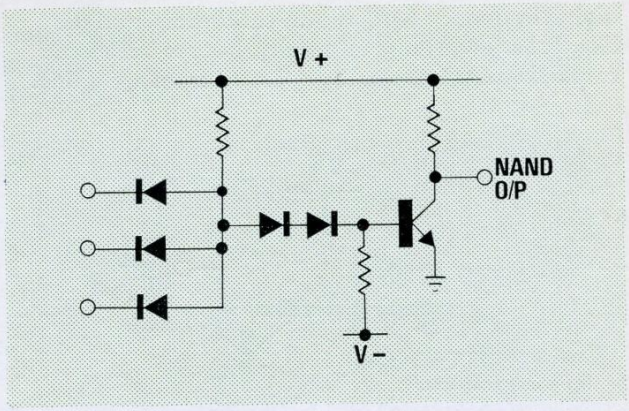


Fig.2. Circuit configuration of a diode-transistor-logic (DTL) device.

RTL (resistor-transistor-logic)

This is a low-to-medium speed family which became very popular in early days of IC digital logic. It is typically operated from 3·0 to 3·6 V supplies; also called DCTL (direct-coupled transistor logic) or (with a speed up capacitor) RCTL (resistance-capacitance transistor logic.)

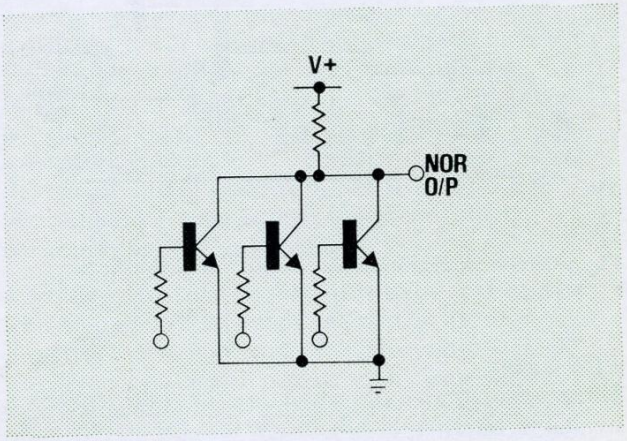


Fig.3. Circuit configuration of a resistor-transistor-logic (RTL) device.

TTL (transistor-transistor-logic)

Sometimes called MEL (multi-emitter-logic), this has been developed for higher speed applications and has become very popular for such applications as

digital frequency synthesisers, calibrators, and the like. It has good noise immunity, but requires some care in layout. It is usually operated from a 5 V line.

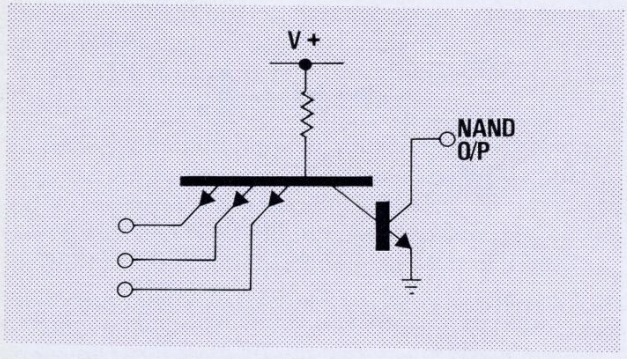


Fig.4. Circuit configuration of a transistor-transistor-logic (TTL) device.

ECL (emitter-coupled-logic)

Sometimes called CML (current-mode-logic), this is a very high speed system with propagation delays to under 10 ns, but provides only a relative low voltage swing and is susceptible to noise. It is usually operated from a 5·2 V line.

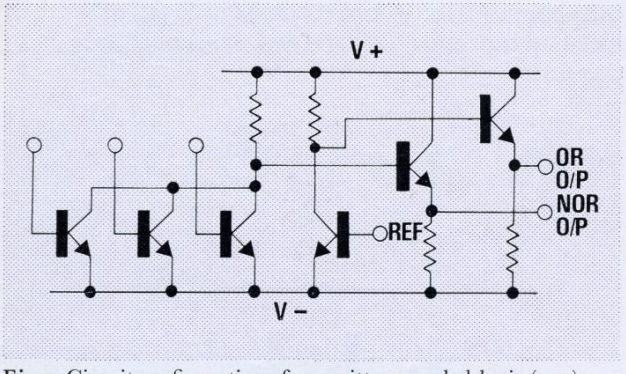


Fig.5. Circuit configuration of an emitter-coupled-logic (ECL) device.

FET Gates

Integrated-circuit gates based on MOSFET devices are available, offering the advantage that the active devices provide the functions of both switching and load resistance. Complementary MOS gates (COS/MOS) combine a mixture of p and n-channel devices to form gates, inverters, counters, flip-flops, and memories. They require extremely low standby power. The following table is representative only and devices may vary significantly from the figures given:

Summary of Gate Properties

	RTL RCTL	*DTL*	*TTL*	*ECL*
Basic function	NOR	NAND	NAND	NOR
Typical max. speed	5 MHz	10 MHz	20 MHz	40 MHz
Voltage swing	2–3 V	5 V	5 V	0·7 V
Noise immunity	Low	Mod-erate	Mod-erate	Low
Power	Low	Mod./ high	High	Mod./ high

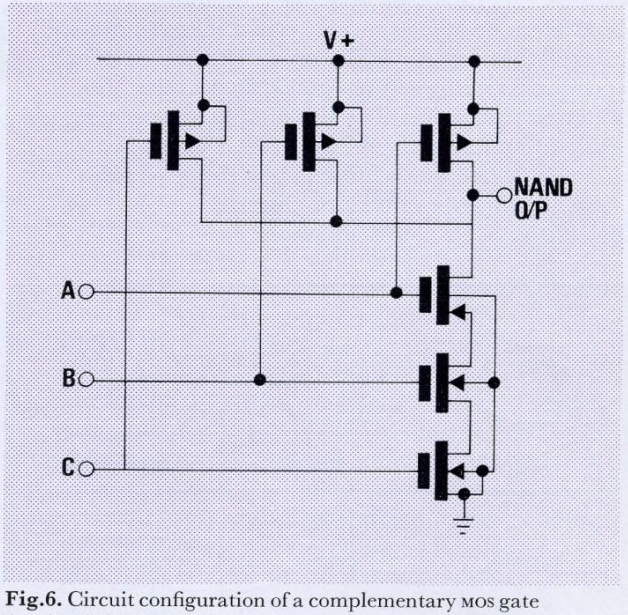


Fig.6. Circuit configuration of a complementary MOS gate (COS/MOS) device.

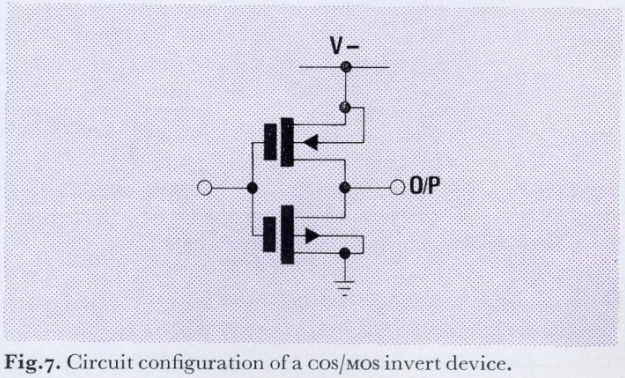


Fig.7. Circuit configuration of a COS/MOS invert device.

PULSE MODULATION TECHNIQUES

During the mid-thirties, at the time when engineers were developing microwave radio communication systems, it was appreciated that there would be advantages if the signal could be transmitted as a series of pulses rather than as a continuous analogue signal. This led rapidly to the development of various modulation systems which would allow the basic intelligence, in analogue form, to be transmitted in pulse waveforms by *sampling* the signal at discrete intervals and then varying or modulating a parameter of the pulses. Techniques proposed included pulse amplitude modulation (PAM); pulse width (or duration) modulation (PWM, PDM); pulse position modulation (PPM); and pulse code modulation (PCM).
In *pulse amplitude modulation* (PAM) the amplitude of the pulse is increased or decreased about a reference level to a degree determined by the amplitude of the intelligence signal and whether it is of positive or negative polarity.
In *pulse duration modulation* (PDM) – alternatively known as pulse width modulation (PWM) – the duration of the pulses increases or decreases around a reference figure.
In *pulse position modulation* (PPM) the precise starting time of the pulses is advanced or delayed by the input signal.

Pulse code modulation

In all the above systems, the fidelity of the signal recovered is determined by the accuracy of the reference amplitude, distortion or time. To obtain the full benefit of a pulse system it is desirable that the only important factor to be determined at the distant end is the simple presence or absence of the pulses. If this can be done then the ruggedness of a basic 'on-off' telegraph system can be achieved in which very considerable distortion of the signalling pulses can be tolerated without introducing errors since a replica of the original pulse can be regenerated locally; further it becomes possible to take advantage of many forms of error detection and correction.
This is achieved in pulse code modulation (PCM) and some of its derivatives such as differential pulse code modulation. In PCM the sample of the information to be transmitted is first converted to the nearest of a fixed number of discrete 'levels'. Each of these levels is allotted a 'code' group consisting of pulses or the absence of pulses. For example, if a binary six-digit code is to be used, the sequence 000001 might indicate 'level 1', 000010 level 2, 000011 level 3, and so on, up to 111111 which would respresent level 63. The coded signal is then transmitted in digital form, for example 1 could be represented by a pulse, 0 by the absence of a pulse.

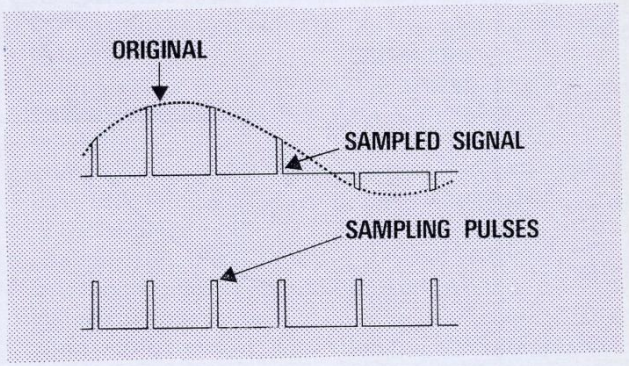


Fig.8. A process is shown for sampling a continuous signal of limited bandwidth. If the analogue signal is connected to a load through a switch which makes contact for short periods at relatively long intervals, then the output will be a train of pulses, as shown above, whose envelope is the original signal. The output is termed a sampled signal.

The coded group or word, on receipt, is 'decoded' to determine the correct 'level' and a signal representing this level is generated, the series of words providing the equivalent of an analogue signal. With PCM, unlike the analogue forms of pulse transmission, the information received is restricted to a fixed number of discrete levels and there is thus an inherent distortion which is termed *quantization noise*. By increasing the number of levels – that is by increasing the number of bits in each word – quantization noise can be reduced to any desired figure. The important advantages of PCM are its exceptionally low susceptibility to noise, interference and distortion of the signals during transmission or storage, and the ease with which the waveform can be regenerated accurately at intermediate points.

The PCM system was devised in 1936 by A H Reeves who soon appreciated that 'it could be the most powerful tool so far invented, against the effects of interference on speech transmission – especially on long routes with many regenerative repeaters, since these devices could easily be designed and spaced so as to make the noise nearly non-cumulative. It was not until about 1947–8 that practical implementation of speech transmission by PCM was attempted, and then – with only thermionic valves available – it still seemed unlikely that it would ever be widely used; it was the invention of the transistor, and later the semiconductor integrated circuit, that radically

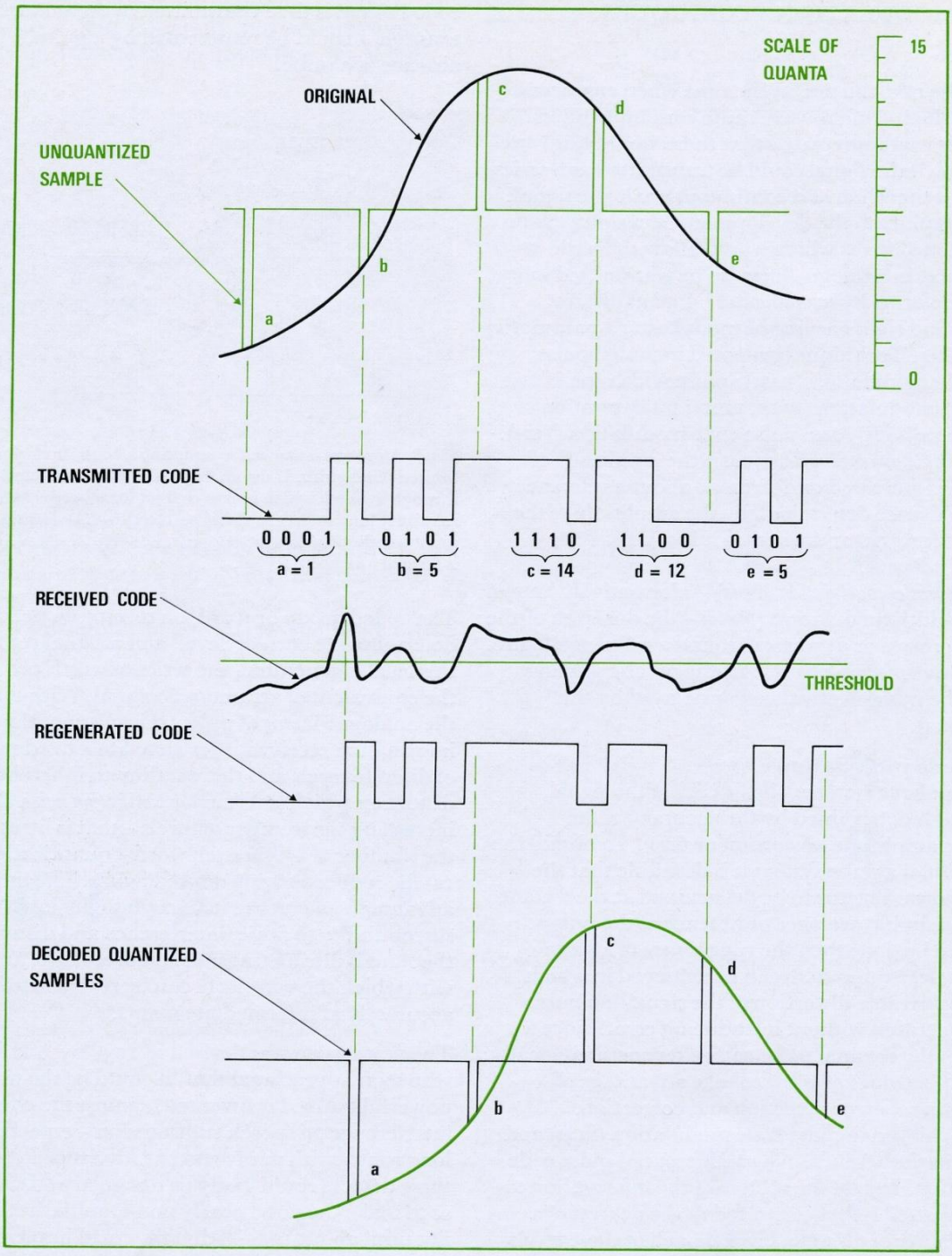


Fig.9. The various waveforms of a digital coding transmission system are shown; a four-digit binary number code is used to convey 16 quantized levels. The received code has suffered considerable distortion but is regenerated by sampling the received code at the centre of each digit period, and generating a transition of appropriate sign; thus it is delayed by half a digit period. Decoding cannot be effected until all the digits have been received so the reconstructed samples are further delayed by a character period. The delays are small enough to be unimportant.

changed the position, making available the switching devices in large numbers that are required for PCM systems. The semiconductor is an almost ideal device for the switching and digital logic operations required in PCM encoding, transmission, regeneration, and decoding. PCM is also highly suitable for time division multiplexing.

The bit rate required for PCM is a function of the number of discrete levels and the sampling rate, and these in turn depend upon the maximum frequency to be transmitted. Good 'telephone quality' speech (about 300–3400 Hz, harmonic margins of 26 dB and signal-to-noise ratio of better than 40 dB) is typically sampled 8000 times a second, coded into seven or eight-bit words to provide 128 levels. A typical 24-channel PCM system, including synchronizing time slots, would have an overall bit rate of 1·6 Mb/s.

For broadcast high-quality music, with a frequency response to 15 kHz and signal-to-noise ratio better than 70 dB, the BBC-developed system using a sampling rate of 32 000 times a second, a 14-bit word (13 information bits plus a parity bit) and a 13-channel time-multiplexed system has an overall bit rate of 6·336 Mb/s.

A high-quality television system would require a bit-rate exceeding 100 Mb/s.

The transmission of high-speed bit streams requires substantial bandwidth. Fourier's theorem shows that any repetitive waveform is composed of a sinewave and a number of harmonics. If the waveform comprises pulses of short duration or short rise or fall times, it must contain higher harmonics. This means that the transmission of high speed pulses *without distortion* requires an extremely wide bandwidth. However for PCM transmission, considerable distortion of the waveform can be tolerated, without degrading overall quality; the bandwidth can thus be significantly less than the theoretical figure. For example, the 24-channel telephone systems, with a bit rate of 1·6 Mb/s, operate over normal paired audio cables with repeater/regenerators spaced at 2000 yard (1·83 km) intervals.

In this volume of the *IBA Technical Review* a number of authors show why digital techniques based on PCM systems are of great potential value to television engineering and outline some of the present and future possibilities; but it is worth emphasizing that the use of PCM is growing rapidly in all areas of telecommunications. The reasons for this have been summarized by K W Cattermole roughly as follows:

a. transmission and storage quality almost independent of distance and network topology;
b. increase in capacity on existing telecommunications cables;
c. compatibility of different traffic (encoded speech, telephone signalling, digital data, encoded television);
d. compatibility of different media (cables, radio links, switching equipment can be interconnected without decoding);
e. present economies in certain applications (e.g. inter-exchange urban junctions, television standards conversion);
f. future economies in system design (for example due to the compatibilities mentioned above);
g. future economies in manufacturing (standardized circuits, mainly digital, in integrated form);
h. possibility of novel facilities (such as encryption, storage, digital processing); and
i. applicability to future transmission media (multiple access space satellites, waveguides, optical fibre and laser systems).

A number of these factors are valid 'here and now'; others need to be taken into account in planning systems for the near future; virtually none is now speculative. The combined weight of these factors, to further quote K W Cattermole, 'is such that most students of the subject are convinced of the value of an extensive digital communication network'.

A Standards Converter Using Digital Techniques

by J L E Baldwin, A D Stalley and H D Kitchin

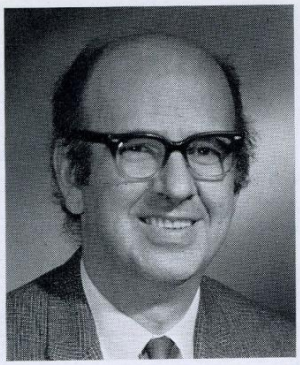
Synopsis

By the autumn of 1969 the IBA was concentrating a good deal of attention on the question of automation, mostly in areas which are not relevant to this article. What is relevant is that the IBA became interested in handling video signals in digital form. It soon became apparent that once the signal had been converted to digital form many different kinds of operation could be achieved using combinations of four basic 'building blocks': *a* a gate, i.e. a word switch: *b* a word adder; *c* a word inverter (to complement data); and *d* a line store; together with suitable ancillaries.

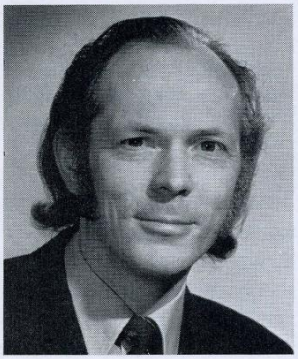
To make these building blocks generally applicable, they were designed to be capable of operating at a word rate equal to three times the colour subcarrier frequency, that is 13.3 megawords per second. This word rate is high enough to satisfy the basic 'sampling theory' requirements of sampling at least twice in each cycle of the input signal.

It was necessary to select a project in order to provide an opportunity for the basic building blocks to be tested operationally. Clearly it would be an advantage if this project could be difficult enough to present a realistic challenge, yet not impossibly so. Further, it should be so chosen that the advantages of using digital techniques could, provided that the project proved successful, be apparent to a considerable number of people outside the research team; this would be achieved more readily if, in practice, the analogue equivalent were only marginal in performance or reliability.

All these pointers made the obvious and natural choice a standards converter.



JOHN BALDWIN, BSc, MInstP, joined the IBA in 1967 to head the new Video and Colour Section; previously he was Chief Engineer with Peto Scott. His career has also included a term with Rank Cintel where he played a major part in developing the only all-British broadcast video tape-recorder. In 1973, with his team, he received the Geoffrey Parr Award and the Pye Colour Television Award for his work on digital television standards conversion. He is a graduate of Norwood Technical College and Battersea Polytechnic; he lives in Croydon, his birthplace, and is married with two children.



TONY STALLEY, BSc (Eng), CEng, MIEE is Deputy Head of the IBA's Colour and Video Section. He is a graduate of the University of Southampton, and before joining the IBA in 1967 he was with the BBC's Research Department, where his work included research into colour techniques and television standard converters; his career has also included work on airborne military equipment with EMI. A Somerset man, he now lives with his wife and two children in Surrey.

HARRY KITCHIN, CEng, MIERE, started his career working on television receiver development with the Thorn Group. He then worked for a time for The Marconi Company, and in 1970 joined the Colour and Video Section of the IBA as a senior engineer. He has now returned to The Marconi Company as manager of the transmitter department in the Broadcasting Division. A Yorkshireman by birth, he is married with one son.

As a first step, the simplest form of standards converter was chosen – a line-standards converter to change a 625-line input signal to a 405-line output. This choice was further governed by the fact that the existing 37 analogue electronic line-standards converters used by the IBA were becoming obsolescent and might need to be replaced in a few years' time.

A theoretical study of a line-standards converter using digital techniques was completed in June 1970. Work began during October 1970 and an experimental digital line-standards converter was demonstrated to delegates of the EBU Technical Committee and to others in March 1971. As a result of the success of this project, a decision was made to develop a field-rate digital standards converter (DICE).

Interpolation

A knowledge of the technique of interpolation is essential to the understanding of the process of standards conversion. Figure 10 shows a much magnified 625-line raster (full lines) while superimposed on this is a similarly magnified 405-line raster (dashed lines). To give some idea of the scale of the diagram, in approximate terms the area shown in the diagram represents a two-thousandth part of the picture area. The points N, O, P, and Q are four points on the input raster, and I is a point on the 405-line output raster. All these points are on a single vertical line.

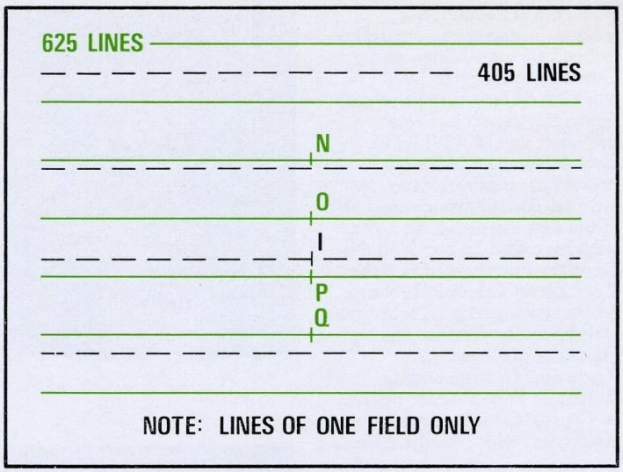
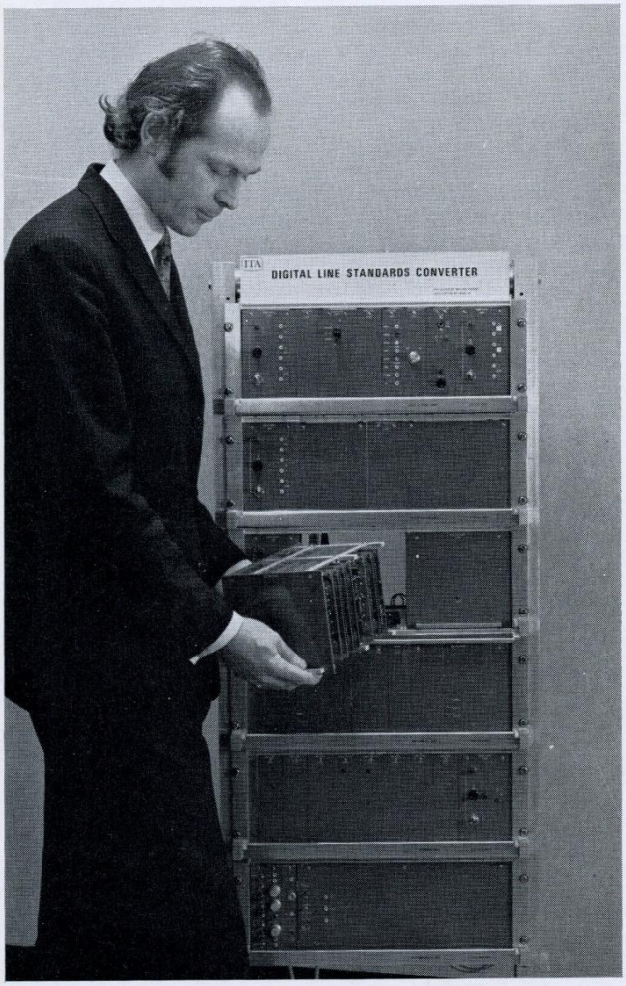


Fig.10. The relative scan structure of 625-line rasters (much magnified). Superimposed is a similarly magnified 405-line raster. The points N, O, P and Q are four points on the input raster and I is a point on the 405-line output raster. All the points are on a single vertical line.



The Experimental Digital Line Rate Standards Converter

The smooth curve of Fig. 11 shows the signal amplitude that might be obtained when scanning down the original scene along the vertical line joining the points N, O, P, and Q. Since the smooth curve does not exist in practice, the required amplitude at point I must be derived from the amplitude at two or more of the points N, O, P, and Q. This simplified explanation indicates why interpolation is necessary in standards conversion and indeed largely describes the process. It may be defined here as the process by which the signal amplitude at a point is derived from the amplitude of a number of points around it–in this case all the points are on one vertical line.

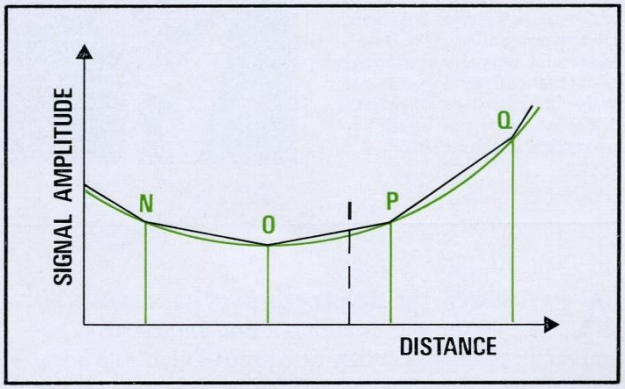


Fig.11. This is an example of linear interpolation and indicated why interpolation is necessary in standards conversion. It shows the signal amplitude that might be obtained when scanning down the original scene along the vertical line joining points N, O, P, and Q of Fig. 10.

One process which could be used would be to assume that the signal could always be determined by the intercept at I of the straight lines joining O and P. However, an error will be introduced which clearly is likely to be greatest half-way between O and P; in practice another disadvantage of this technique will become apparent later on.

Figure 12 shows how the required proportions of the two signals vary as the point I moves from O to P. At O, the proportion of the P signal is zero, as shown, and it rises linearly to unity as the wanted position of I moves towards P. At the same time the required proportion of the O signal drops from unity linearly to zero. The dotted lines in the diagram indicate how to obtain the proportions of the two signals for a particular position of I.

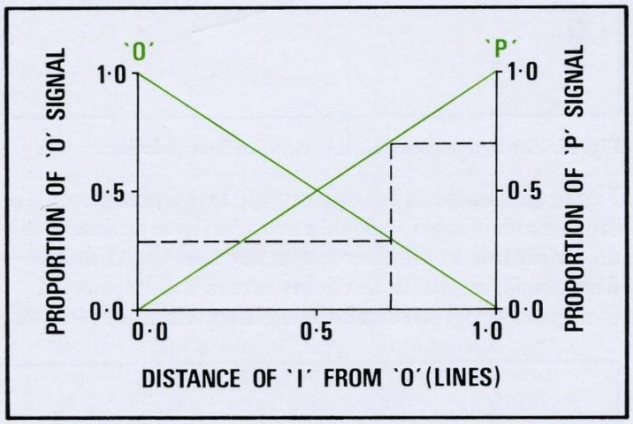


Fig.12. This shows how the required proportions of the two signals vary as the point I moves from O to P. The dotted lines show how to obtain the proportions of the two signals for a particular position of I.

If I happens to fall at either O or P, then only one signal is used to form the wanted signal. At these points the resolution remains unimpaired. At all other points between O and P an addition of two spatially separated signals is used and this must inevitably cause a loss of resolution.

This is shown in Fig. 13 which includes a small vector diagram showing how, in the general case, the resultant falls short of the low-frequency response, where ϕ is clearly zero. Since ϕ is proportional to frequency, the horizontal axis of the graph may be considered to represent frequency. Two cases are shown. These are the extremes: one being where the required output coincides with an input line, e.g., I coincides with O; the other case is where the output position is midway between input lines, equal

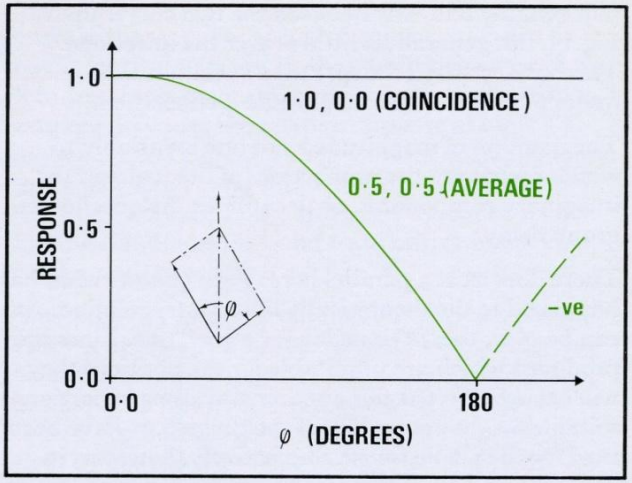


Fig.13. This shows how at all points between O and P an addition of two spatially separated signals is used. This inevitably causes a loss of resolution. The vector diagram shows how the resultant falls short of the low frequency response, where ϕ is clearly zero.

proportions being taken. This diagram thus indicates that large variations of frequency response occur, depending on the proportions of mixing of the two signals.

One possible way of minimizing this effect would be to limit the range of proportions that can be used, as shown in Fig. 14. The range of proportions has been restricted to one-quarter to three-quarters of each of the two signals. Naturally it still includes the same midway position (so the frequency response of that condition will be unchanged) but the frequency response of the other limiting case is not shown. It

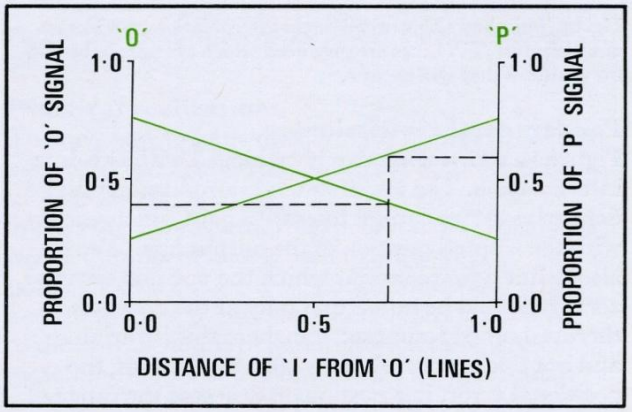


Fig.14. Large variations of frequency response occur; depending on the proportions of mixing of the two signals. This can be minimized, as shown here, by limiting the range of proportions that can be used. The range is restricted to one-quarter to three-quarters of each of the two signals.

falls roughly half-way between the two curves in Fig.13, but generally a little nearer the lower one. This has decreased the spread of variation with frequency, in so far as magnitude is concerned.

The mention of magnitude leads one invariably to wonder what are the proportions of the real and the imaginary components, or to consider the question of group delay.

There does exist a parallel here: Fig.15 shows what has happened to the theoretically linear interpolation. As can be seen, the 'fit' is no longer a good one. Lines are produced which are unsuitable for the positions they will occupy. To put this another way, the proportions suitable for the centre half of the range O, P, have been used for the whole range. Subjectively, however, it does give slightly better results – at least in some respects, though worse in others – than simple linear interpolation. But this is clearly not satisfactory, and it appears sensible to look carefully at fundamentals.

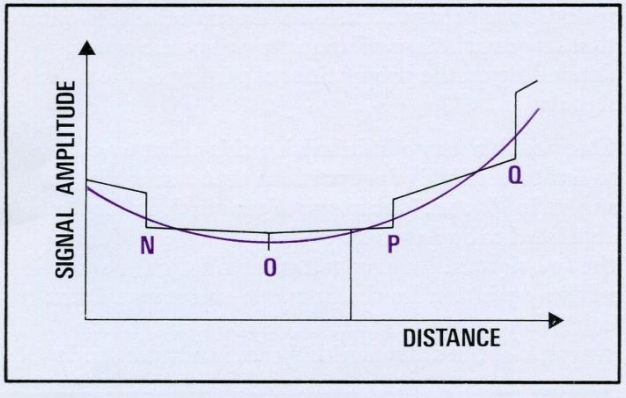


Fig.15. This shows how raised linear interpolation provides an unsatisfactory 'fit'. Lines are produced which are unsuitable for the positions they will occupy.

Fundamental restrictions

Figure 16 shows what can be achieved with two-line interpolation. The low-frequency amplitude must be defined since we cannot tolerate a gain which varies with the wanted position of the output line. We can also define a frequency at which the position error is zero. It should be noted that only at the crosses is there a defined response: elsewhere this is variable and not under control. However, by ignoring the positional error, it is possible to decrease the range of the amplitude/frequency response.

Obviously, more degrees of freedom are required. To avoid carrying out a similar analysis for each possible system, let us consider the four-line case, as shown in

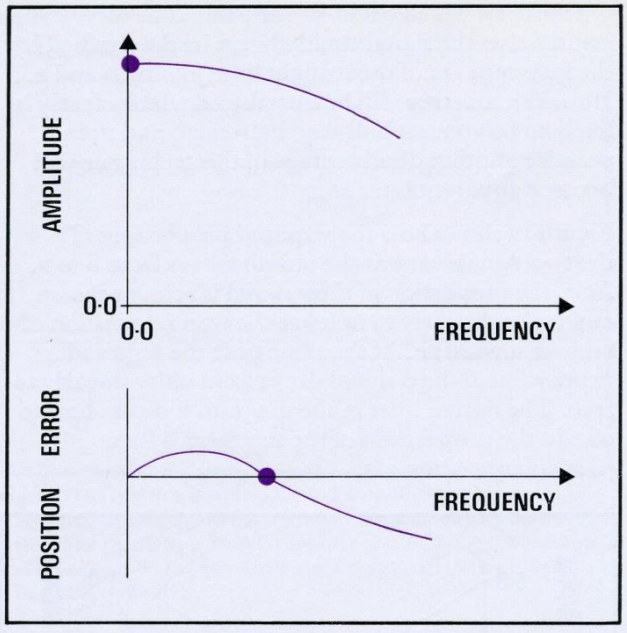


Fig.16. The design constraints of two-line interpolation.

Fig.17. In addition to defining the low-frequency amplitude, it is also possible arbitrarily to define an amplitude at another frequency and to define two frequencies at which the delay errors will be zero. A computer program has been written which accepts the

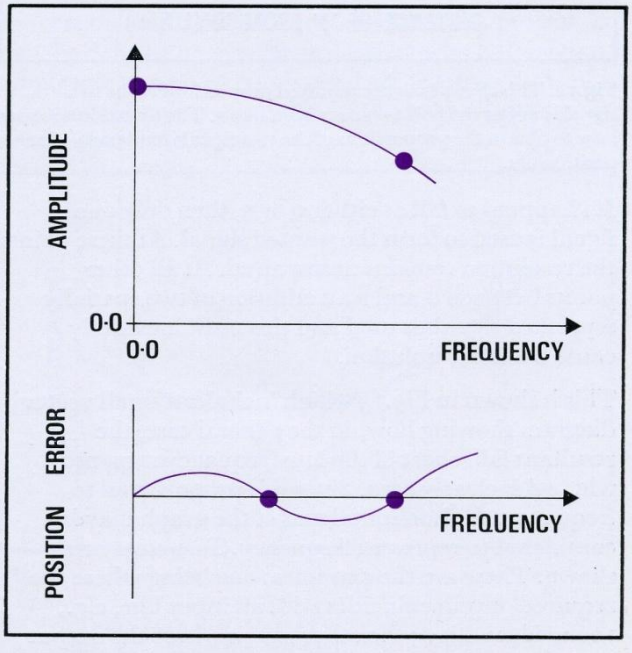


Fig.17. The design constraints of four-line interpolation.

desired constraints and produces a print-out of the required proportions against relative positions of the wanted output line. For a particular choice of constraint values, Fig.18 shows how the relative proportions of the four signals vary as the wanted line moves in steps from one coincidence point to the next.

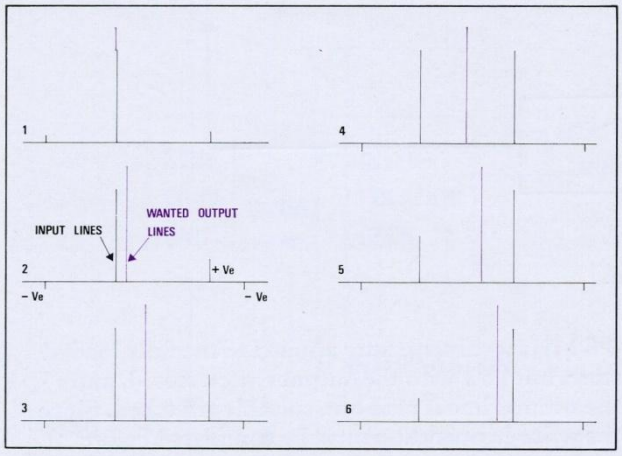


Fig.18. This shows six sets of four-line interpolation coefficients. The relative proportions of the four signals vary as the wanted line moves in steps from one coincidence point to the next.

Both of the upper two sub-diagrams of Fig.18 show symmetrical cases, and it is worth contrasting these two conditions. In the coincident case (left-hand sub-diagram) the two adjacent small contributions decrease the response at high frequency relative to that at low frequencies. In the condition shown in the right-hand sub-diagram, however, the two negative components cause the relative response at high frequencies to be greater that it would be owing to the centre pair alone, and this tends to equalize the frequency response of the two cases. It can be seen that the sub-diagrams 5 and 6 are mirror images of 3 and 2 respectively.

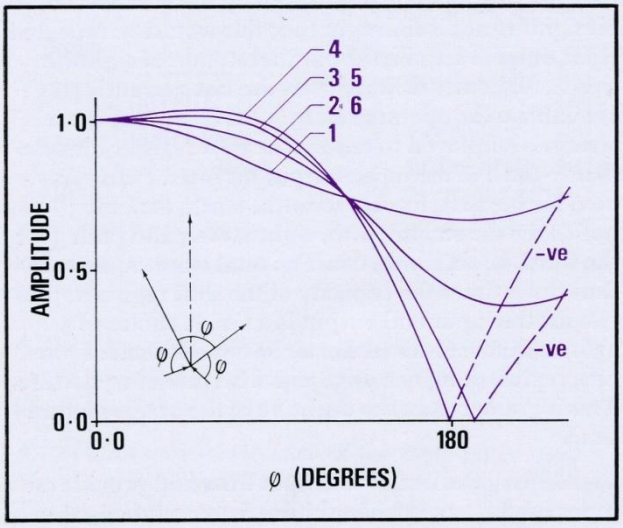


Fig.19. The frequency response obtained using the sets of interpolation coefficients of Fig.18 is shown. This indicated the responses going through a common point at about 120°.

The frequency response obtained by these coefficients is shown in Fig.19. This indicates the responses going through a common point at about 120°. In addition, the change of frequency response with change of wanted position has been significantly reduced, when compared with the two-line case shown in Fig.13. Figure 20 shows the overall shape of an interpolation function spanning four lines.

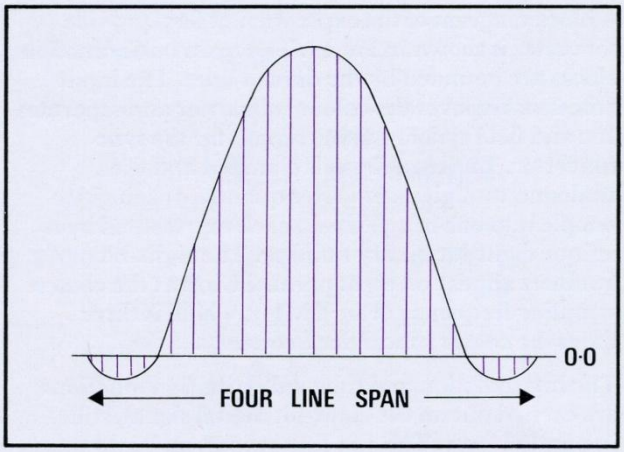


Fig.20. This shows the overall shape of an interpolation function spanning four lines.

Practical realization

Turning now to some details of the approach we have adopted Fig.21 shows the basic function blocks needed for line-standards conversion. The video signal follows the upper path. Interpolation of vertical detail over a number of lines is used to improve the portrayal of sloping edges. Time distribution is needed to space evenly the wanted lines according to the output standard and to stretch those lines to match the longer active line time. The sync signals are separated from the composite input signal and follow a different path through the converter. In the sync conversion unit a sync pulse train is generated appropriate to the output standard, together with timing waveforms controlling all other functions in the converter.

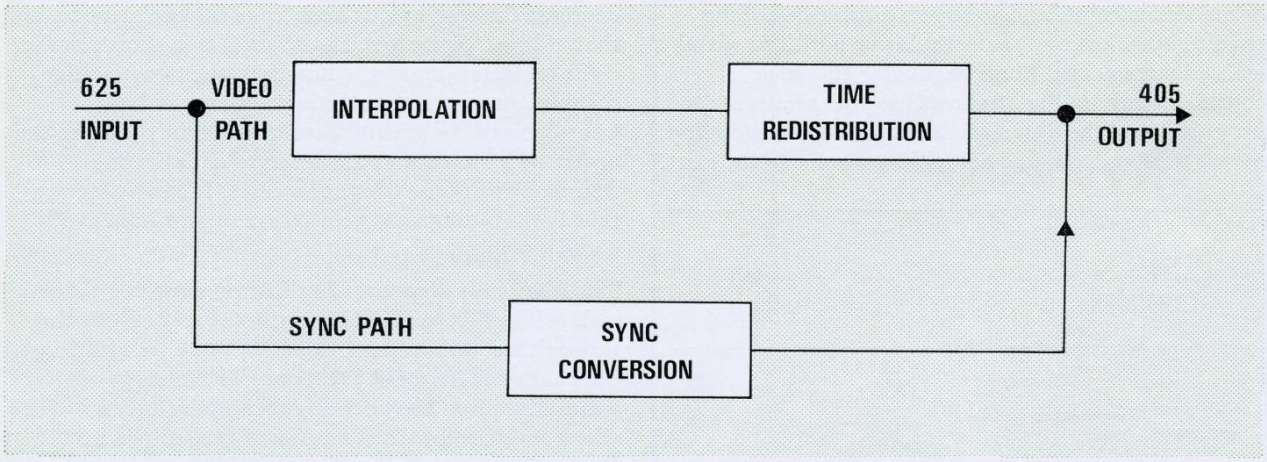


Fig.21. The basic function blocks needed for line-standards conversion.

A block diagram of the experimental 625/405-line converter is shown in Fig.22. The main basic function blocks are bounded by the dashed lines. The input processor removes the colour subcarrier and separates line and field synchronizing signals for the sync converter. The black level is clamped and the analogue-to-digital converter quantizes each video sample into one of 256 levels, each represented by a unique eight-bit binary number. The eight-bit numbers appear on eight parallel wires at the chosen sampling frequency of 13·3 MHz, which is three times the colour subcarrier frequency.

The interpolation and time redistribution functions are carried out on the eight-bit digital signal, still in parallel form. The 405-line output, owing to the stretching of the active line period, appears at an 8·6 MHz rate. The parallel eight-bit output is converted back to an analogue waveform by the digital-to-analogue converter. An output processor filters and blanks the video signal, and inserts a 405-line sync waveform produced by the sinc converter.

Time redistribution

Figure 23 shows the time redistribution process in greater detail. In computer terminology this would be known as a 'buffer store'. In fact it consists of three stores, A, B, and C, wired in parallel, with input and output switches selecting the wanted paths. Each store consists of 'serial-in serial-out' shift registers of the correct length to hold one picture line. A wanted line of the input standard (625-line) is 'written' into an empty store by applying the correct number of 13·3 MHz shift pulses with the appropriate input switch closed. The same number of pulses, but at 8·6 MHz is subsequently applied to the fully loaded store, but now with the output switch closed, and the wanted line is read out, suitably stretched. Since the write-in operation must be completed before read-out can ensure that an empty store is always available at the start of a wanted line. The input and output 'enable' pulses and 'read/write' shift pulses are supplied by the store control in accordance with the wanted-line sequence determined in the sync converter.

One-line digital store

The block diagrams of an eight-bit, one-line store is shown in Fig.24. The path taken by the least level of bit significance is shown in full; this would be repeated eight times to handle the parallel stream of eight-bit words. Since MOS shift registers are not currently available to be operated at 13·3 MHz, a three-path system is employed to reduce the shift register bit rate to one-third of the input-output bit rates. Path 1 is used for the first, fourth, seventh, tenth, etc., bits; path 2 for the second, fifth, eighth, etc.; and path 3 for the third, sixth, ninth, etc. The total store capacity is thus three times the capacity of the shift registers, plus two for the input and output latches. A choice of a 256-bit shift register makes a convenient total of 770 bits, representing nearly 58 μs at a bit rate of 13·3 MHz. This is greater than the duration of the active picture time.

Eight AND gates buffer the input lines and provide an input inhibit; 24 latches, shift registers, and wired-OR gates respectively demultiplex, store and re-multiplex the eight-bit streams; eight tri-state latches retime the output words and provide an output 'disable'

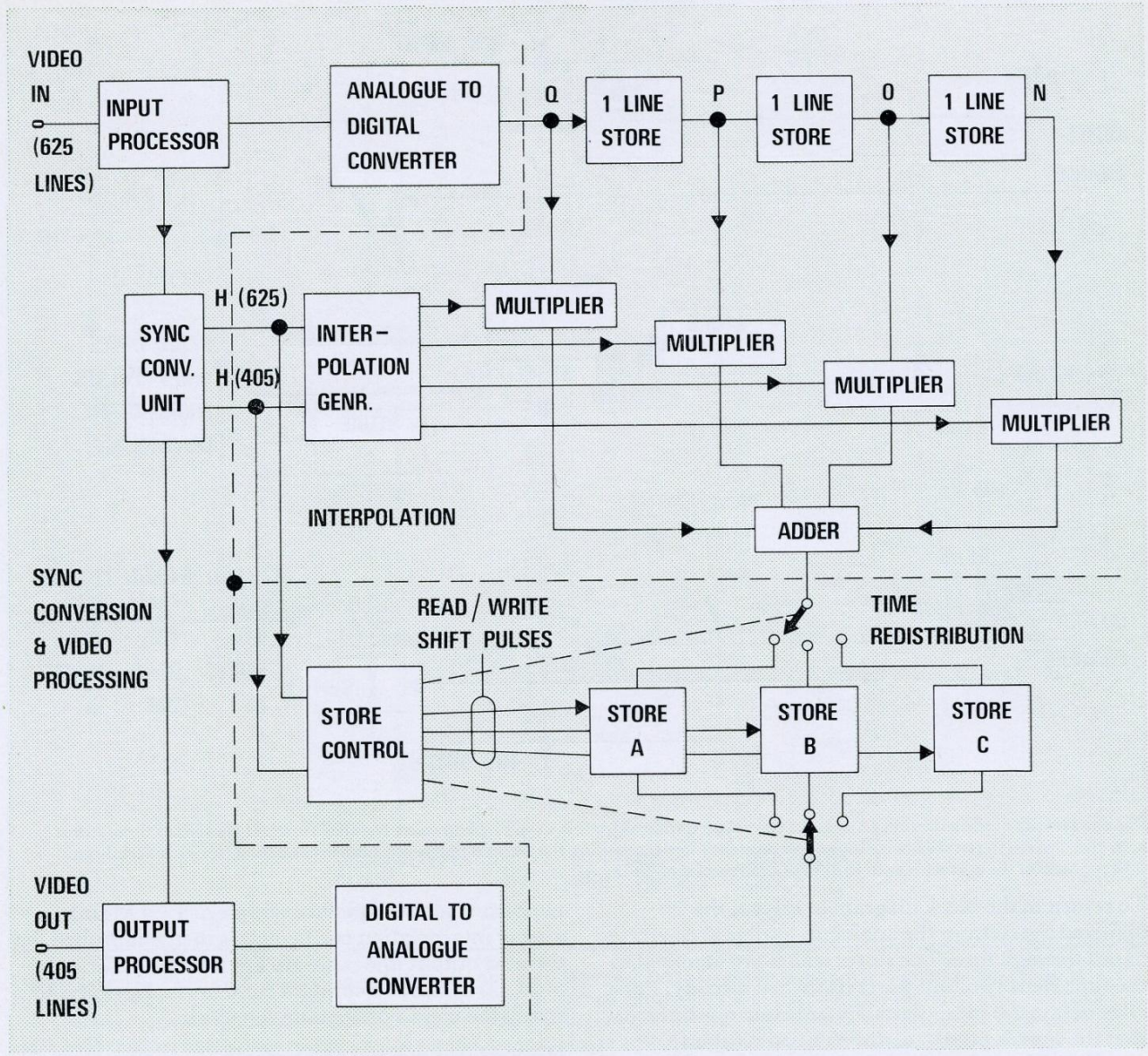


Fig.22. Block diagram of the IBA's experimental 625/405-line digital standards converter; indicating how the basic functions are achieved.

facility. Fortunately, all the necessary devices are available in quad packages, thus reducing the number of integrated circuits required to 22.

As the shift registers in each of the three paths need biphase shift pulses, a total of six phases are required. The store is therefore assembled with a companion board carrying a six-stage ring counter. This divides down from the input clock pulses at the data rate, and drives six push-pull amplifiers supplying 17 V shift pulses to the highly capacitive MOS shift registers. The peak shift currents are of the order of 0·25 A, so the layout of the components must be arranged with care. Other clock pulses on the store board are provided by suitably decoding the ring counter so that only one input clock line to the module is necessary.

Four-line interpolation

It is necessary, at this stage, to consider the interpolation processes actually used in the converter.

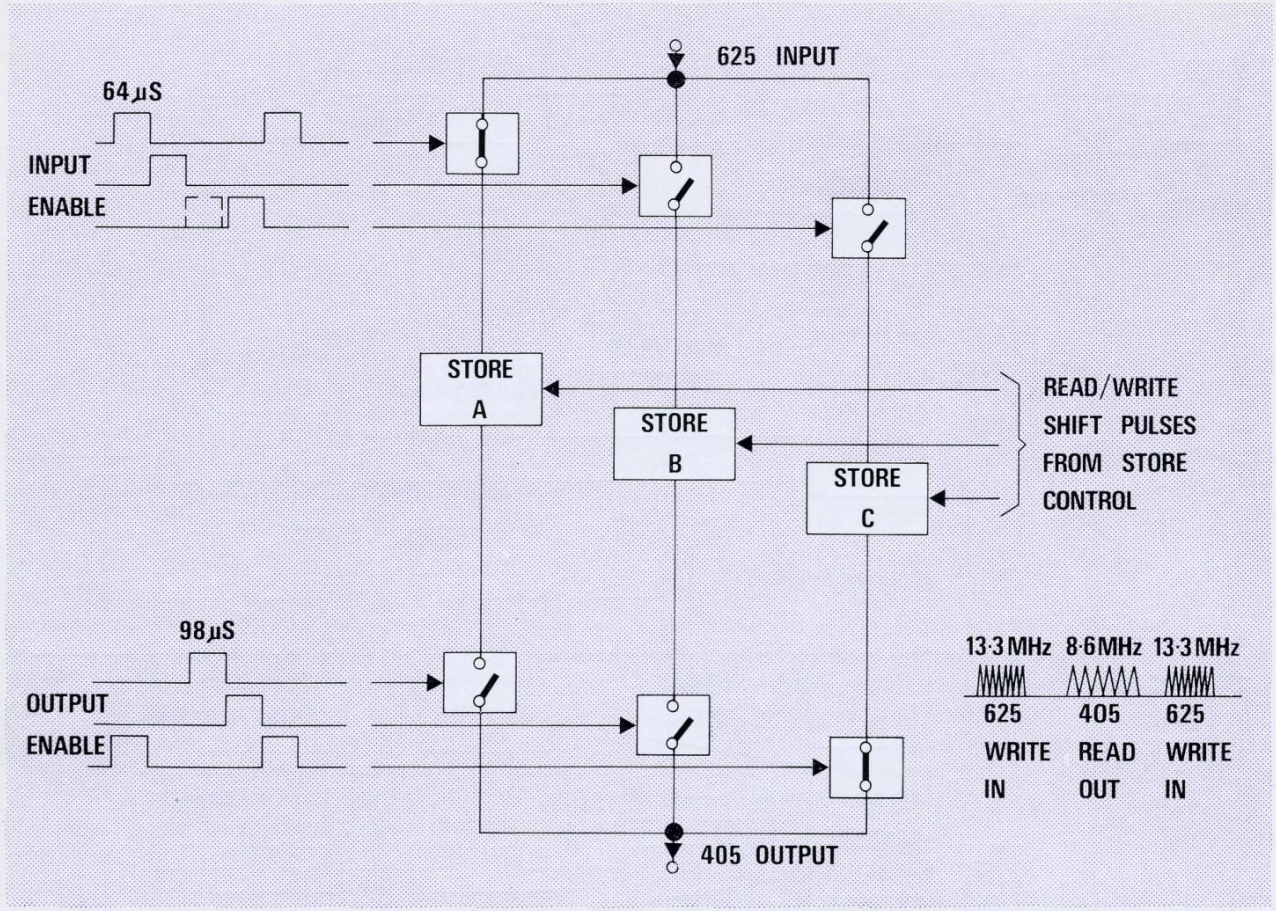


Fig.23. The time redistribution process. In computer terminology this would be known as a 'buffer store'. It consists of three stores A, B, and C wired in parallel, with input and output switches selecting the wanted paths. Each store consists of 'serial-in serial-out' shift registers of the correct length to hold one picture line.

To return to the block diagram of Fig.22, the digitized signal from the analogue-to-digital converter passes through three line stores which are identical to the time redistribution stores described already. Each store delays the input signal by precisely one line, so that the signals at Q, P, O, and N, at any instant, represent four vertically displaced points on the adjacent lines of a given field. In Fig.25 the signal amplitudes at the four points are e_1, e_2, e_3 and e_4. The interpolated amplitude to suit an output line position as shown is e_{out}. For the symmetrical example chosen, the interpolation function would call for equal contributions from e_2 and e_4 to enhance the vertical definition. The multiplying coefficients might be, say, $-0{\cdot}1$, $+0{\cdot}6$, $+0{\cdot}6$ and $-0{\cdot}1$. The four multipliers calculate four products: $-0{\cdot}1e_1$, $0{\cdot}6e_2$, $0{\cdot}6e_3$ and $-0{\cdot}1e_4$, and these are summed to provide the interpolated output e_{out}. These calculations are performed for each picture sample at 13·3 MHz; a set of interpolation coefficients is then established for the next output line position. Each set of coefficients must always have a constant sum, normally unity, to satisfy the condition for a uniform field.

High-speed binary arithmetic

Figure 26 shows an example of the multiplication of two four-bit binary numbers. As with decimal multiplication, the multiplicand is staggered one place for multiplication by each successive digit of the multiplier. With a binary multiplier consisting of only 'ones' and 'zeros', the staggered multiplicand is simply counted or ignored. Summing the four rows give the product. Summing pairs of rows and then adding the totals clearly give the same answer. Binary multiplication amounts to addition of staggered versions of the multiplicand, where each staggered version counted corresponds to a one in the multiplier.

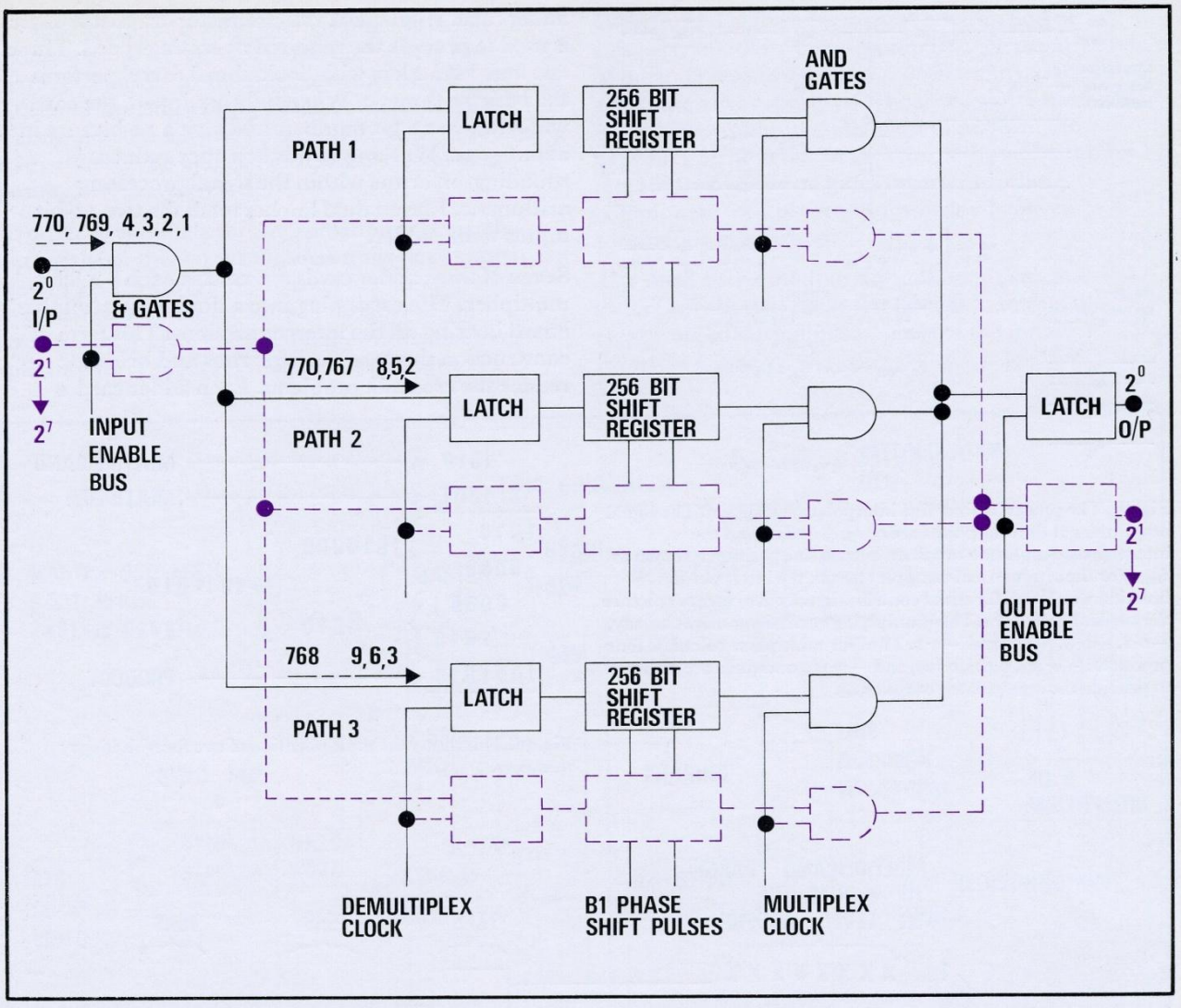


Fig.24. This shows a block diagram of an eight-bit, one-line store. The path taken by the least level of bit significance is shown. Path 1 is used for the first, fourth, seventh, etc. bits; path 2 for the second, fifth, eighth, etc. and path 3 for the third, sixth, ninth, etc. The total store capacity is thus three times the capacity of the shift registers, plus two for the input and output latches. A choice of 256-bit shift register makes a convenient total of 770 bits, representing nearly 58 μs at a bit rate of 13·3 MHz. This is greater than the duration of the active picture time.

Figure 27 extends this principle to show an 8×8 bit multiplier as used in the experimental converter. It uses seven adders. The multiplicand is wired in a staggered fashion to the inputs of the first four adders; in practice each adder input being preceded by a latch. Where a zero occurs in the multiplier, that row of latches and thus the adder inputs, is reset to zero. All other latches feeding first-level adders hand on the multiplicand when they receive a clock pulse. The four first-level additions then start, and are complete before the next clock pulse transfers those four numbers to the two second-level adders. Similarly those two answers are available before the next clock pulse starts the final addition. The 8×8 bit multiplication is therefore complete within three clock periods, but proceeds continuously at the 13·3 MHz clock rate.

All the 'arithmetic' in the converter – addition, subtraction and multiplication – is built from a basic

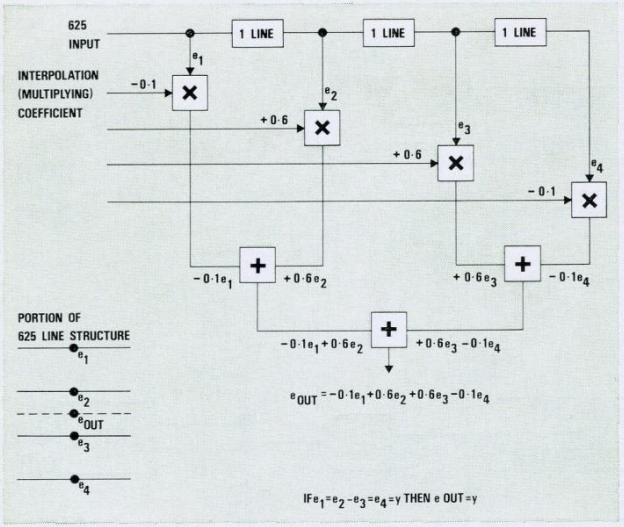


Fig.25. The process of four-line interpolation is shown. The signal amplitudes at the four points are e_1, e_2, e_3 and e_4, and the interpolated amplitude to suit an output line position is shown as e_{out}. For the symmetrical example chosen, the interpolation function would call for equal contributions from e_2 to e_4 to enhance the vertical definition. The multiplying coefficients might be, say, $-0{\cdot}1$, $+0{\cdot}6$, $+0{\cdot}6$ and $-0{\cdot}1$. The four multipliers calculate four products: $-0{\cdot}1e_1$, $0{\cdot}6e_2$, $0{\cdot}6e_3$, and $-0{\cdot}1e_4$, and these are summed to provide the interpolated output e_{out}.

adder card. High speed TTL (transistor-transistor-logic) is used to provide the required operating speed. Three fast four-bit adders with 'look-ahead carry' perform the basic arithmetic. When fully equipped, the card will add two 11-bit numbers and give a 12-bit sum in about 40 ns. Working to this accuracy reduces rounding-off errors within the signal processing arithmetic. Eleven dual latches latch the two 11-bit inputs to the adder.

Seven of these adder cards are used in each 8×8 bit multiplier. The cards plug into a double-side 'mother' board bearing all the interconnections. This form of construction shortens the logic runs and helps to reduce the crosstalk problems. Each adder card is

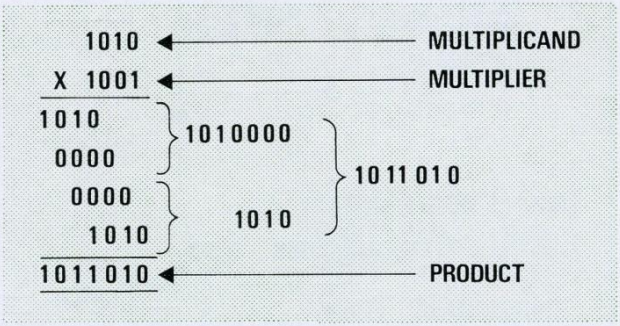


Fig.26. This shows the multiplication of two four-bit binary numbers.

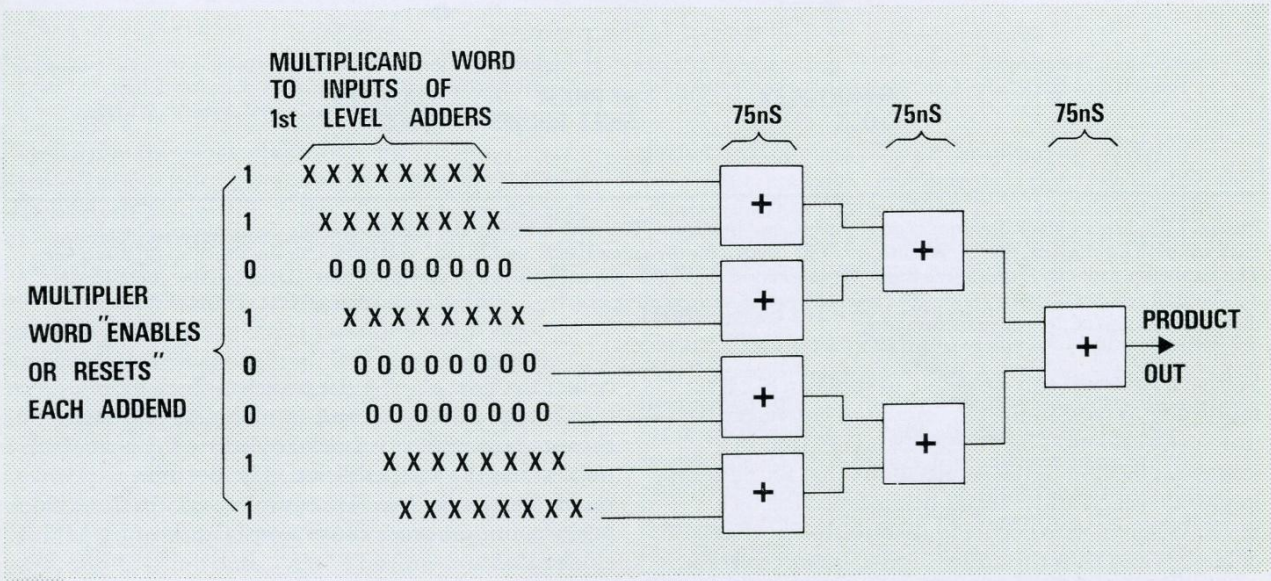


Fig.27. This shows fast binary 8×8 bit multiplication as used in the experimental converter. It uses seven adders and the multiplicand is wired in a staggered fashion to the inputs of the first four adders, each adder input being preceded by a latch. Where a zero occurs in the multiplier, that row of latches and thus the adder inputs is reset to zero.

equipped with only sufficient packages to match the significance of its position in the multiplier. In spite of this economy, the module consumes about 4 A when multiplying at 13·3 MHz. A useful service feature is that a fully equipped card can be kept as a spare that can be plugged into any of a total of 31 positions in the converter.

In order to complete the interpolation process, the outputs from the four multipliers must be summed: see Fig.22. However, the division into modules had to take into account the limited number of pin connections and for this reason the adder block was split into three separate modules as shown in Fig.25.

Clearly, two of the adders must have an add or subtract capability to accommodate the negative lobes of the interpolation function. Both inputs to the third adder are always positive. The three adder modules use the basic plug-in adder card to perform the necessary arithmetic. In the case of the add/subtract modules, exclusive OR gates invert, or rather compliment, one of the input words whenever subtraction is required.

The third adder module is almost identical, and differs only in that it has fast latches to retime the eight wanted output bits in place of the input inverting gates.

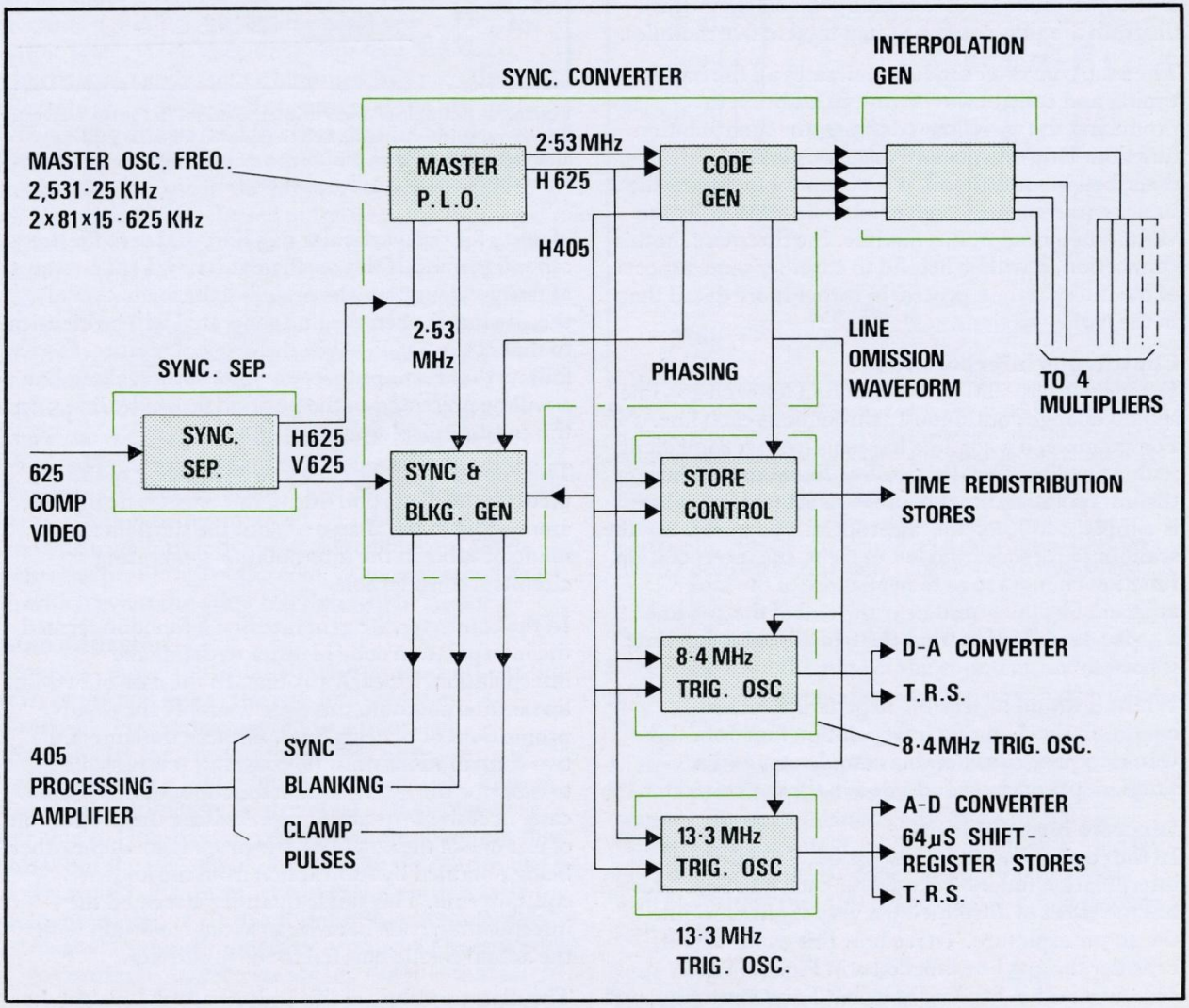


Fig.28. A block diagram showing the main processes of the sync conversion process.

The adder output still has the timing of the 625-line signal, but now contains information appropriate to a 405-line structure as a result of interpolation. Time redistribution then completes the digital processing needed to convert the signal.

Sync conversion

If we refer again to Fig.21 it will be noted that the term 'sync' conversion is used to cover those parts of the converter concerned with providing the various waveforms needed to drive the digital and analogue circuits. This process is shown in more detail in Fig.28 where the enclosing lines show the grouping of the functions to form the plug-in modules for sync conversion, green lines indicate the different modules. The eight functions identified by the blocks in this diagram are thus contained in a total of five modules.

The sync converter module generates all the basic timing and control waveforms, in addition to producing the waveforms defining the interpolation function. However, before this module can be described in some detail, it is necessary to discuss the basic requirements which need to be fulfilled by the various functions in this module. Furthermore, in this connection, it will be helpful to consider some aspects of the interpolation process in rather more detail than in the earlier sections.

Continuous interpolation

For ideal interpolation, the function for each 405 line should change continuously throughout each line. For example, if a 405 line happens to start coincident with a 625 line, then for two-line linear interpolation, the interpolation function at the start of the 405 line is simply 100% of the appropriate 625 line. As the scanning proceeds from left to right, the interpolation function changes so as to need more of the lower adjacent 625 line, until near the end of the 405 line a 50:50 contribution from the two adjacent 625 lines is necessary.

Whilst it would be feasible to generate such a continuously changing interpolation function, this would require considerable complexity, and a simpler approach was adopted in the IBA converter.

Discrete interpolation

In the equipment under discussion, a fixed-value interpolation function is used for each 405 line. This has the effect of introducing a very slight skew into the 405-line picture. To see how this comes about, consider the 405 line labelled A in Fig.29. This coincides with a 625 line at its left-hand extremity, and thus requires at this point an interpolation coefficient

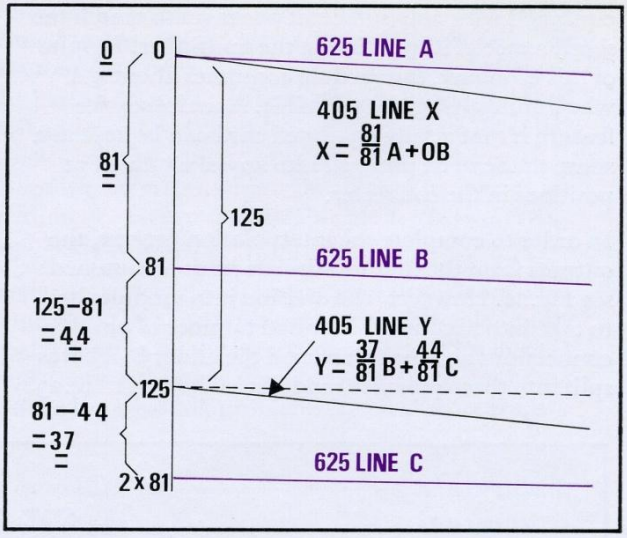


Fig.29. An example of discrete interpolation. In the IBA converter a fixed-value interpolation function is used for each 405 line although as can be seen this has the effect of introducing a very slight skew into the 405-line picture.

of unity for this particular 625 line, and zero for the other 625 lines. If this coefficient is now kept constant at unity throughout the period of the formation of the 405 line X, then the line generated will be identical to that of the 625 line A in the original picture. It follows that the input picture information along line A will be presented in the position shown by line X on the 405-line display.

This represents a slight clockwise skewing of the picture; the distortion due to this effect is negligible, amounting to less than 0·1°, but the simplification made possible in the interpolation generating circuits is considerable.

In the converter, we generate first a function termed the interpolation code in order to define the interpolation, for each 405 line. In the case of two-line linear interpolation, this code is simply the relative proportions of two 625 lines. Because the sum of the two contributions must be constant, it is possible to describe the interpolation function, in this simple case, by a single quantity representing the proportion of just one of the 625 lines, the proportion of the other being obtained by subtraction from the known constant sum. This single quantity is termed the interpolation code in order to avoid confusion with the actual coefficients fed to the multiplier.

The discrete values of this code, for each line, can be seen in Fig.29 by considering the relative positions of

the input and the output lines of the picture along a vertical line to be that formed by the left hand side of the picture. An enlarged section of the superimposed input and output displays in this region is shown in the diagram.

Since the numbers 405 and 625 are each divisible by five, the basic relationship between the two systems is the ratio 81 :125. If the space between two adjacent 625 lines is divided into 81 divisions, and this scale is continued, then the space between two adjacent 405 lines will contain 125 divisions. The equations in Fig.29 give the proportions of the two adjacent lines required to form a correctly interpolated 405 line.

This diagram may also be thought of in terms of the time domain, with the left-hand vertical lines as a time scale; it then becomes apparent that the interpolation code can be obtained by ascertaining the state of a divide-by-81 counter, at the instant when a 405 line starts. However, this technique would give the code values at the 405-line rate, and is thus not suitable for use in the present converter where all interpolation is effected at the 625-line rate. It is essential, therefore, to create the interpolation code at the start of each 625 line. Thus, for instance, at the start of line B, we need to know that the code value for the 405 line Y is 44. This is achieved by employing a divide-by-125 counter and ascertaining its state at the start of each 625 line. The count remaining gives the required code value. In the example shown, for line Y the count remaining is 44, which is thus the required interpolation code. The proportions of the 625 lines are thus 44/81 for C and 37/81 for B, the latter fraction being obtained by subtracting the first one from unity. By using this technique, there exists the possibility of the code value exceeding 81, in which event the other fraction will be negative.

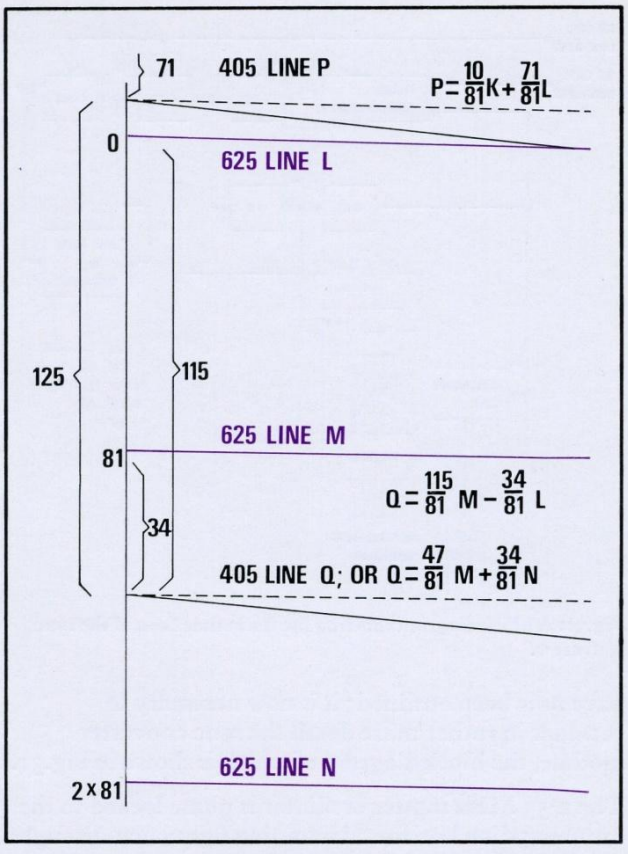


Fig.30. The principles of the line omission technique are shown. At the start of the 625-line L, the remainder in the divide-by-125 counter would be 115 so that the line formed should be made up of 115/81 parts of M and minus 34/81 parts of L. This would ultimately be stretched and displayed as 405-line Q. Preferably, however, line Q should be formed from immediately adjacent lines M and N. Accordingly all interpolated 625-lines where the remainder exceeds 81 are omitted prior to time redistribution.

Line omission

Figure 30 shows the situation when this occurs. At the start of the 625 line L, the remainder in the divide-by-125 counter would be 115 so that theoretically the line formed should be made up of 115/81 parts of M and minus 34/81 parts of L. This line would ultimately be stretched and displayed as 405 line Q. However, it is clear from this diagram that this is not the best choice for forming the output line Q, and it would, in fact, represent extrapolation rather than interpolation. Instead, line Q should preferably be formed from the immediately adjacent lines M and N. Accordingly, in this case we use the rule that all interpolated 625 lines where the remainder exceeds 81 are omitted prior to time redistribution.

The waveform defining the omitted lines can easily be derived from the state of the counters, and is used to inhibit the interpolation and the time redistribution 'write' operations.

In the design of the experimental IBA converter it was not considered necessary to use all 81 different values of the interpolation code. Instead, only 27 distinct values are used, each one of which is used for three of the possible 81 code values. Practical tests have confirmed that this degree of resolution is more than adequate.

Sync converter

The basic principles involved in the generation of the interpolation code and the line omission waveform

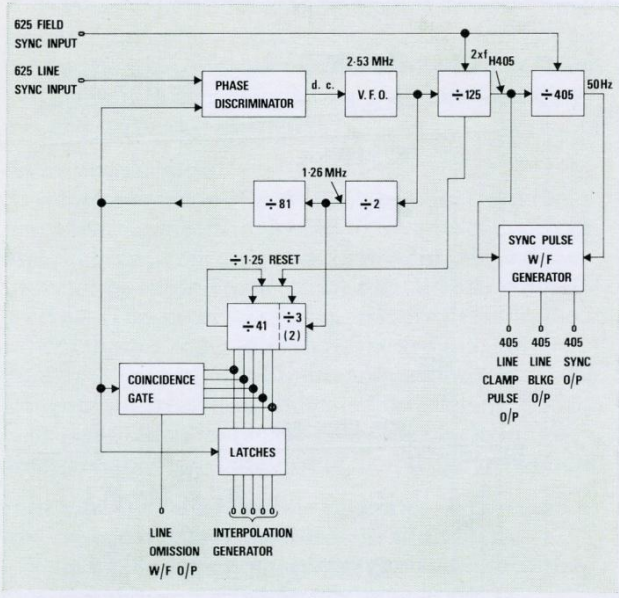


Fig.31. A block diagram showing the main functions of the sync converter.

have now been outlined; it is now necessary to consider in rather more detail the sync converter module, the block diagram of which is shown in Fig.31.

The 2·53 MHz master oscillator is phase locked to the input 625-line horizontal scanning frequency through the divide-by-2 and the divide-by-81 counters. The output from the divide-by-2 stage yields a 1·26 MHz pulse train; 81 cycles of this make up one 625-line period so that it becomes the time domain equivalent to the spatial divisions mentioned above. These pulses are fed into the divide-by-125 counter which is made up of an eight-stage binary chain, with the first two stages connected to divide by three. An overall reset is provided when the count of 125 is reached. By taking the output from the six later stages, which effectively form a divide-by-41 counter, the division of the 81 values by three is accomplished, thus yielding 27 distinct interpolation codes. The state of the counter is sampled at the 625-line rate and stored for the duration of each 625 line in the output latches.

The line omission waveform is obtained by the separate gating and latch circuit shown on the left-hand side of Fig.31. Also included in this diagram are the divide-by-125 and divide-by-405 counters used for the generation of the 405-line sync, blanking and clamp pulse waveforms. The 625-line input field pulse from the sync separator is fed into those counters and ensures that they are set correctly at the start of each field. A further feed is taken from the divide-by-125 counter in the sync chain to the divide-by-125 interpolation code counter to ensure that the code values are generated in phase with the 405 sync and blanking waveforms.

Interpolation function generation

The 5-bit interpolation code signal from the sync converter has to be translated into four eight-bit coefficients, in accordance with the chosen interpolation function. These coefficients are then fed to the four multipliers. To provide flexibility in the choice of interpolation function, the translation from the code to the coefficients includes a diode pin matrix.

Because the interpolation function is invariably symmetrical it is possible to represent the 27 interpolation code values by a mid point value, and 13 other values, each of which occurs twice. Thus a matrix with 14 columns is adequate. Each column of the matrix contains points of intersection with 32 horizontal rows grouped into four banks of eight, to give four outputs of eight bits for the four multipliers. Diode pins are inserted at the intersections in a pattern derived from the chosen interpolation function. The use of this arrangement makes it possible to assess rapidly the effectiveness of a variety of interpolation functions. In a converter designed solely for operational use such a refinement would be quite unnecessary, and the translation from the interpolation code to the interpolation coefficients would be fixed to provide optimum subjective results.

Size of equipment

The experimental IBA digital converter occupies only 42 in. of rack height, made up of six 7 in. panels. One contains the video processing and sync conversion circuits. A second panel houses power supplies and the interpolation function generator. Two further panels are occupied by the arithmetic modules; the fifth contains six line-stores, and the sixth panel houses the analogue-to-digital and digital-to-analogue converters. In a production model, the height occupied by the converter could almost certainly be reduced to 35 in. or less.

Conclusions

Compared with the analogue type of line-standards converters currently in service, it can be shown that the performance of this type of digital converter is generally superior. The use of digital techniques has eliminated the majority of preset controls that would

otherwise be necessary, and has also enabled the proportion of discrete components to be decreased by about four-fifths. As a result of these changes, it is expected that the reliability of such a converter would be significantly better; the limited practical experience to date indicates that these expectations will be realized.

The converter was used operationally for a period during the summer of 1971, when it was temporarily installed at the IBA's colour control centre at Croydon, and provided the 405-line signals for the Channel 9 Croydon transmitter which provides VHF service for the entire London region.

This experimental line-standards converter was planned as the first step in the application of digital techniques to standards conversion generally. The results obtained convinced us that this is an appropriate technique for all forms of conversion, and we have subsequently developed the field standards converter DICE which uses many of the same basic techniques. An introduction to DICE is published in this issue.

DICE – Digital Intercontinental Conversion Equipment

Synopsis
The IBA digital field-rate television converter is a compact device occupying no more than two 6-ft equipment racks, which is to be compared with the seven racks of earlier electronic converters. It converts 525-line, 30 pictures-a-second, NTSC colour television signals into 625-line, 25 pictures-a-second, colour-separation (red, green, and blue) signals which are then coded into either PAL or SECAM signals in a normal analogue coder.
The new converter uses digital television techniques and the standards conversion process is to all intents and purposes free of distortion. It uses a number of novel techniques for decoding the NTSC signal and for interpolating between fields and lines.

The earliest type of field converter to be used for changing 60-field signals into 50-field signals was an optical converter which used a camera, operating on one scanning standard, to look at a cathode-ray-tube picture display operating on the other scanning standard. A later development for colour television has been to use two such arrangements, with one camera-to-display unit converting the luminance picture and a second camera-to-display unit converting the coded chrominance signal. In general, optical standards converters have problems with halation, spot-size, lag, phosphor grain pattern blemishes, the compromise between phosphor decay-time and movement judder, chrominance resolution and the registration of the luminance and chrominance signals.

All-electronic analogue converters avoid some of the problems of optical converters but have been, to date, much more expensive, and much larger. If they use quartz-delay lines then the delay-lines need to be operated in a controlled environment to avoid variations in delay-time with temperature, while starting from cold is not practicable. The write-in and read-out rates have to be the same, and organizational problems arise in continually switching between numerous lines of different delay times. Spurious signals in the delay lines cause picture defects, especially on saturated colours, and attenuation in the lines, coupled with the need for amplitude and group-delay equalization, make the devices electrically noisy and tedious to line-up. Since the subcarrier which emerges from the delay-line is used to judge the time delay, the noise on the subcarrier signal limits the timing accuracy of the output. The analogue separation of chrominance and luminance is imperfect and gives rise to further picture defects.

Once the television signal has been converted from its normal analogue waveform to a data-stream of binary digital pulses, considerable improvements can be made in the conversion process. The cost of such complex data processing depends upon the sophistication and technical elegance of the computation logic which is developed, and the present IBA converter is at once notable for the economy of its means and for the precision of its numerical calculation.

The storage elements are – as for the line converter – computer shift registers using MOS FET technology. Such storage of digital data in shift registers is impeccable and there is no degradation of the signal in the store. At the same time, the write-in and read-out rates can be different, and the delay between writing and reading is flexible and can be precise.

The machine has an instantaneous warm-up and there are no preset controls in the digital conversion circuits. A particularly noteworthy feature of the design is the type of spatial filter which is used, among other operations, to produce the luminance, and the I and Q chrominance signals, from the incoming composite data stream. Inherently, the spatial filters have perfect tracking and there are no adjustable controls.

The digital parts of the equipment are designed mathematically for a given performance and they calculate to their design accuracy. Although – as in any equipment – parts can fail, it is not possible for

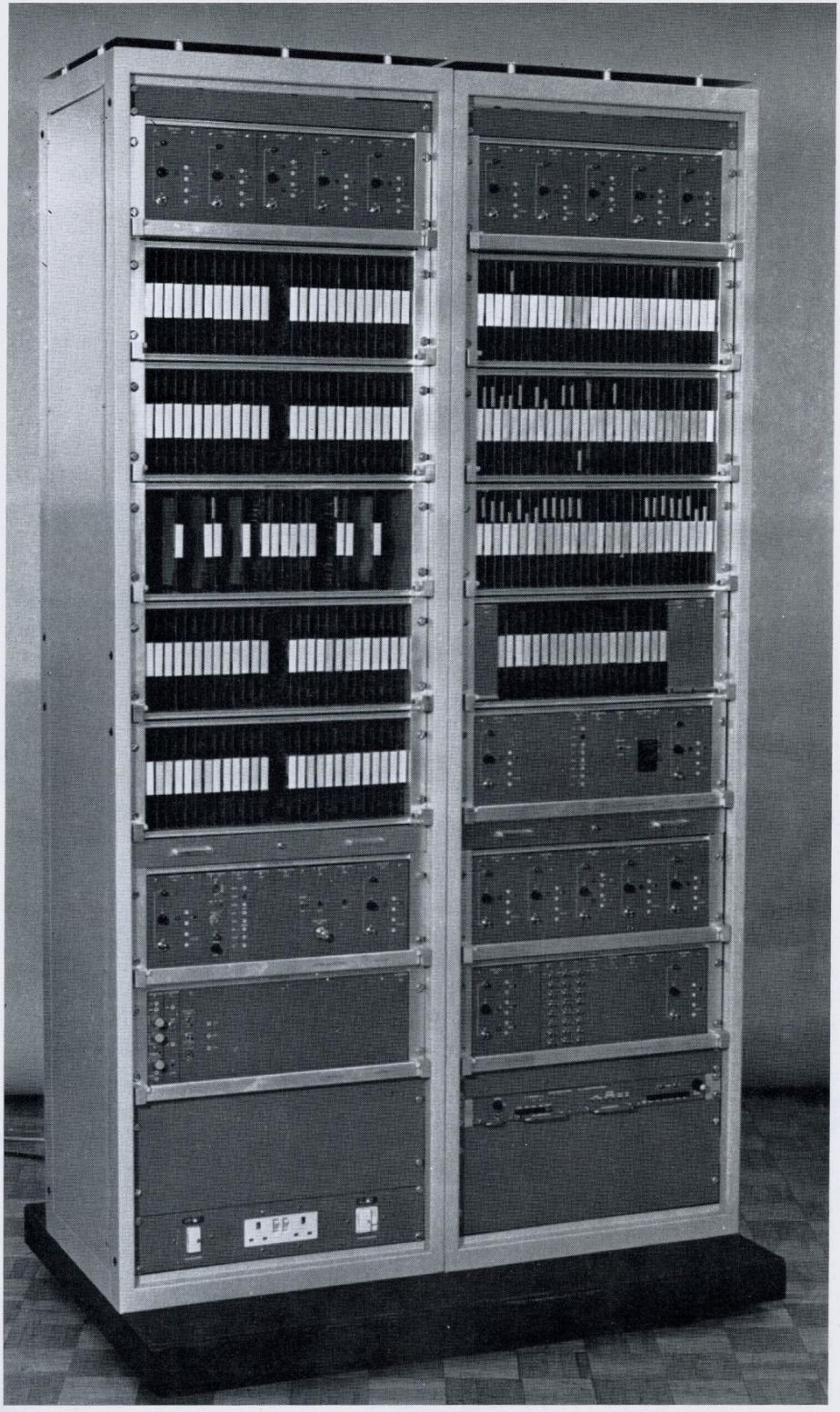


Fig.33. The IBA's digital field rate converter.

the performance to drift away from its design tolerance, and the converter will, for example, always give a *k*-rating factor of better than 1%.

Although the converter uses nearly 8000 integrated circuits and the shift registers represent some 15 million transistors, an important element of the design is the repetition of circuits, ICs and boards, which has reduced costs and simplifies repair work. Most of the circuit boards can be tested on plug-in go/no-go test sets which not only show if a fault is present but also indicate its location. The cost of integrated circuits is falling steadily and the machine should become even cheaper. It represents a further step forward in the IBA's engineering programme which aims to make what is already the most comprehensively equipped colour-television network in Europe, even more cost-effective.

Principles of the field-rate converter

There are three main functions which such a converter has to carry out. It must change the field rate from 60 to 50 Hz (and lengthen the duration of the field period), and it must change from a 525-line scanning rate to a 625-line scanning rate, and it must change both the colour subcarrier frequency and the modulation of the subcarrier.

The operation of the digital field-rate converter will be described with reference to the block schematic of Fig.34. After synchronizing signals have been fed to the timing control circuits, the first operation

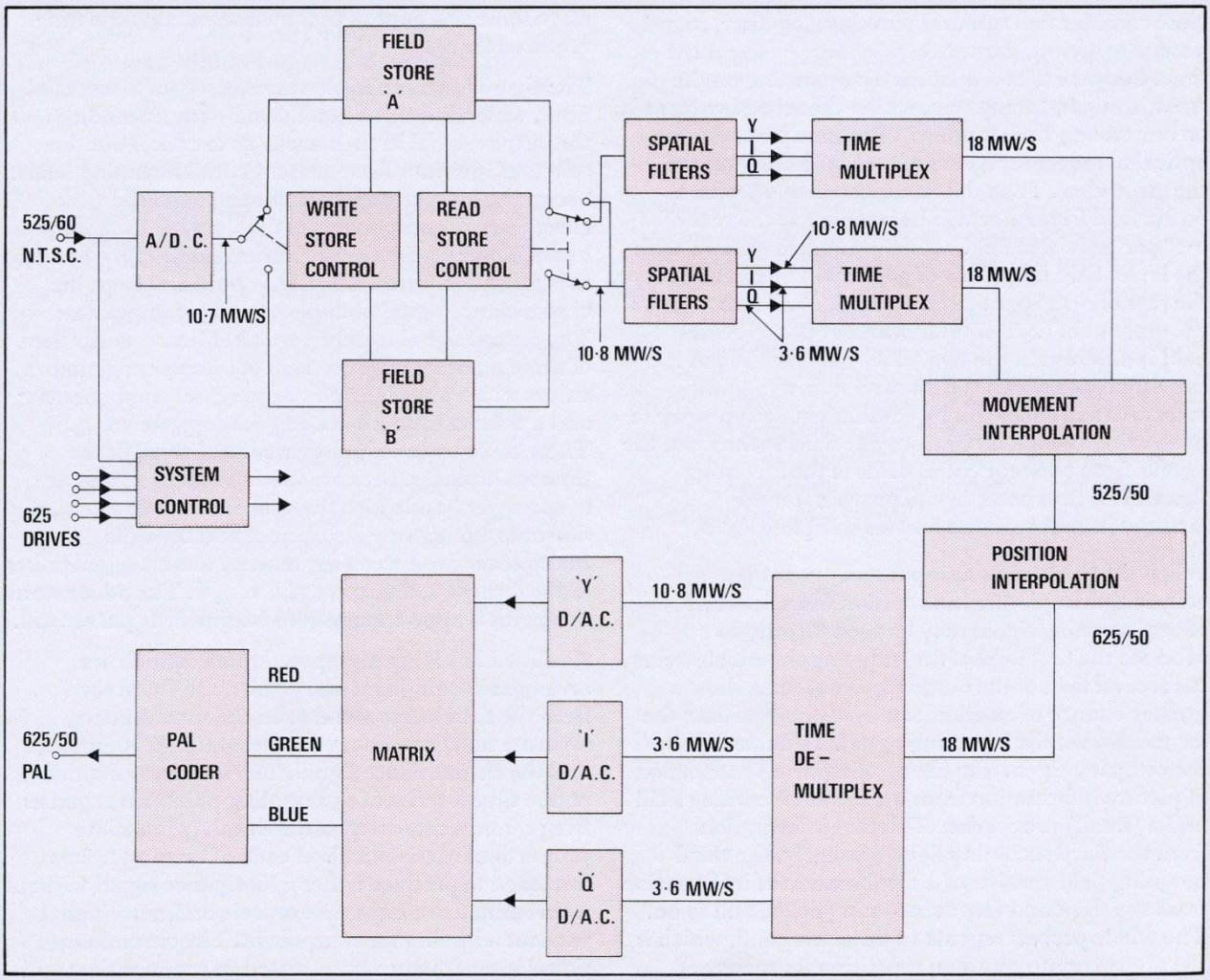


Fig.34. A block diagram showing the basic functions of the converter.

of the converter is to change the incoming coded analogue video signal into a digital signal in an analogue-to-digital converter. The sampling rate chosen is three times the subcarrier frequency (10·7 MHz) since this rate is higher than the Nyquist requirement for waveform accuracy and enables several novel techniques to be used in the subsequent processing. Each picture element so sampled is then analysed into one of 256 equally-spaced amplitude levels to produce an eight-bit binary-coded output pulse-train, or word. To reduce the maximum operating-speed requirement of the solid-state devices in the following circuits, eight-wire parallel circuit feeds are used from this point onwards – and further down the chain this is increased to 24 parallel feeds, and later to 32.

Now consider two cameras panning, together, round a scene at an angular rate of 6° of arc per second of time. Suppose that one camera is operating on the American 525-line system, whilst the second camera is on our UK 625-line standards. Presume that suitable optical arrangements ensure that both cameras see the same view. Then the American camera with a 60 Hz field frequency will be panning at the rate of 0·1° per television field, while the British camera with the lower field frequency of 50 Hz will be panning at the rate of 0·12° per television field. That is to say, the amount of horizontal movement per television field is different in the two television systems and it is this difference which the movement interpolator must create. It does this by combining, in appropriate proportions which differ from one field to the next, the signals from two sequential fields of the incoming signal. It is thus necessary to provide storage facilities in shift registers for two complete fields.

When the fields on both input and output systems coincide, then picture information from field one of the incoming signal may be used directly to produce the first field of the outgoing signal. However, the second field of the outgoing signal must show a greater change of position of moving objects than the second field of the incoming signal. To achieve this, the outgoing signal is made up of a (large) proportion of picture information from the second incoming field and a (small) proportion of picture information from the third incoming field. Similarly, the third outgoing field consists of a combination of information from the third and fourth incoming fields, and so on. The whole process repeats 10 times a second, which is the approximate common repetition frequency of the two standards involved.

Of course, in order for such a combination of signals to be satisfactory, the signal from two sequential incoming fields must at any moment relate to identical picture points. This is not the case when the signal is generated because of the interlaced relationship between succeeding picture fields.

Information is read out of the two field stores simultaneously, at a rate depending on the required outgoing line frequency. Each field store is made up of 48 modules arranged in groups of four and each group of modules stores 21 lines of picture information using a total of 96 shift registers each of 1 024 bit capacity. The outgoing line-time is very nearly the same as the incoming line-time, and the rate is now 10·8 Megawords a second. However, because of the difference in field rate required, there are at this stage some line gaps so that 21 lines occupy the time required for 25.

The signal from each field store then goes to a spatial filter, which has three functions. Firstly, it modifies the output signal in such a way as to cancel out the effects of interlace between sequential incoming fields. Secondly, it separates the luminance and the chrominance components of the signal without any loss of either vertical or horizontal resolution – at any rate for still pictures. Thirdly, it produces from the chrominance signal obtained, I and Q components. The output signal from the spatial filters consists then of three separate parts; a train of luminance signal values Y; a train of chrominance signal components I; and a train of chrominance signal components Q. These three trains of pulses are interleaved in the time multiplexer. Because the I and the Q signals are of narrower bandwidth than the luminance signal, a slower sampling rate is sufficient and the time multiplexer produces a sequence of output signal pulses in the form of Y, I, Y, Q, Y; Y, I, Y, Q, Y. The data rate at this point is approximately 18 Megawords per second.

As shown in Fig.34, the spatial filters, which are arranged as complementary pairs, are fed in turn from the field stores A and B. In the spatial filters, separate matrices are used to generate the luminance and the chrominance signal. The matrices examine at one time a series of 15 sampling points arranged as five points in three sequential lines. Appropriate proportions of the signals at each of these 15 points are taken to produce either a luminance signal without a chrominance component or a chrominance signal without a luminance component. The chrominance signal is separately demodulated to produce the I and Q components.

The movement interpolator takes proportions of each of the multiplexed signals and for every six incoming fields produces the appropriate five outgoing fields. The ratio of the two standards is not precisely 5:6 and the actual operation is somewhat more complex. At the output of this movement interpolator the signal consists of 525 lines of picture, but running at the 50 field rate.

The function of the line interpolator is to generate from these 525 lines, a sequence of 625 lines each with the information appropriate to its position in the picture. This, of course, fills in the line gaps mentioned above.

An interpolation process is again used, the picture points in each outgoing line being produced by selecting appropriate proportion of the corresponding signal points from three incoming lines.
The time demultiplexer separates the luminance pulses from the I and the Q information and each is separately converted back from the digital to the analogue form. The three signals obtained are then matrixed to produce standard R, G, B, signals and the composite colour signal is finally obtained using a standard colour coder, either a PAL coder or a SECAM coder.

Synchronization

As was mentioned above, the reading rate for the field stores depend directly on the outgoing line frequency required. The converter is designed to be locked by station synchronizing signals in the same way as a camera or any other picture source.

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2. J L E Baldwin, A D Stalley, and H D Kitchin, 'A Standards Converter using Digital Techniques', *Royal Television Society Journal*, **14**, No.1, pp.3–11.

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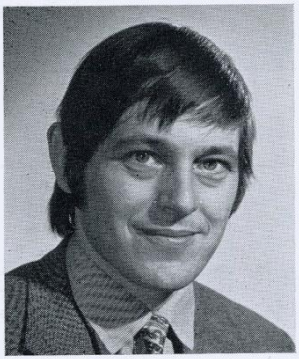
This digital field-rate converter, although designed and built as an experimental model, was acquired early in 1973 by Independent Television News and is now in regular programme service. It was conceived by J. L. E. Baldwin who first sketched out the basic design in the autumn of 1971. A. D. Stalley was responsible for the day-to-day management of the development project; the engineers who were concerned with its development included: H. Kitchin, I. Lever, J. Taylor, J. Coffey, R. Greenfield, P. Owen, P. Mercer, B. Gillings and C. Rowling of the IBA's Experimental and Development Department. It was first demonstrated in September 1972 and two months later was used operationally during the American presidential elections when pictures received at the earth station at Goonhilly were successfully converted and fed to the European networks. Further development is aimed at producing a two-way switchable machine.

The development of this digital intercontinental conversion equipment ('DICE') has been widely recognised as an outstanding engineering achievement. Both the Geoffrey Parr award of the Royal Television Society and the joint Royal Television Society/Pye Colour Television Award 1973 for the 'most significant technical contribution during the year to the development of colour television' have since been awarded to John Baldwin and his team.

PETER HUTT, BA, DIC, joined the IBA in 1970, and since then has worked on automation and digital techniques in the IBA's Experimental and Development Department. A graduate of Cambridge University and Imperial College, London, he started his career working in the Middle East oil industry; prior to joining the IBA he was engaged in research into pcm telephony techniques with the Plessey Company. He is married with two children and lives in London.



A System of Data Transmission in the Field Blanking Period of the Television Signal

by P R Hutt

Synopsis

As part of a broad IBA investigation into the possibilities digital methods present for television engineering, a system has been developed for the transmission of data in the vertical interval of the television signal. The system uses lines 16 and 329 of the 625-line signal and basic design and outline is explained.

The choice of data format and the coding system, together with the factors affecting these, are described. Also considered are the data receiver and the system's error probabilities.

There are many uses to which such a data transmission system can be used, with the information ultimately displayed on a screen. One particular use already being adopted by the IBA is the labelling of programmes with a source identification; such a system has significant benefit in a programme network as complex as the IBA's.

Television engineers have for long been aware of the empty lines at the beginning of every field, and recently there has been a mushrooming interest in the use of these lines for data transmission. If we consider the field blanking portion of the System I signal we see that a total of 50 of the 625 lines standard signal do not convey the picture. In each field 25 lines were initially devoted to field sync and receiver recovery and from lines 6 to $23\frac{1}{2}$ of the first field there are $18\frac{1}{2}$ lines which were specified initially to be at black level.

The general term for any signals transmitted during or on these lines is 'insertion signals'. The first insertion signals to be widely adopted have been International and National Insertion Test Signals on lines 17, 18, 19, 20, and corresponding lines on the second field. (The even field line number such as 16, normally infers also the odd field line number, in this case line 329.)

In 1969 the CCIR set aside line 16 (and 329) for the transmission of data, and the European Broadcasting Union[1] began considering what form these data signals should take and for what purpose they should be used. There are in fact a multitude of possible uses for this data channel and it is important at the outset to ensure that the best possible system of modulation is adopted to satisfy all the possible requirements, transmission conditions and uses that may arise. A system of data transmission has been developed and tested at the IBA which has been the stimulus for similar studies by other EBU organizations. It is hoped that eventual standardization on insertion data signals will be agreed on the basis of this system.

In designing a system of data transmission for use in conjunction with the video signal it is tempting to relate parameters of the data signal to features of the television signal such as line rate, colour subcarrier frequency, leading-edge-of-sync time, etc. However, in order to achieve the most reliable system of data transmission it is of fundamental importance that the data system has maximum independence from any of these parameters. In this way the data system will most often be the last part of the total system to fail in the event of adverse conditions or equipment malfunction.

A data communication system is typically illustrated by Fig.36. In the case of insertion data it is the

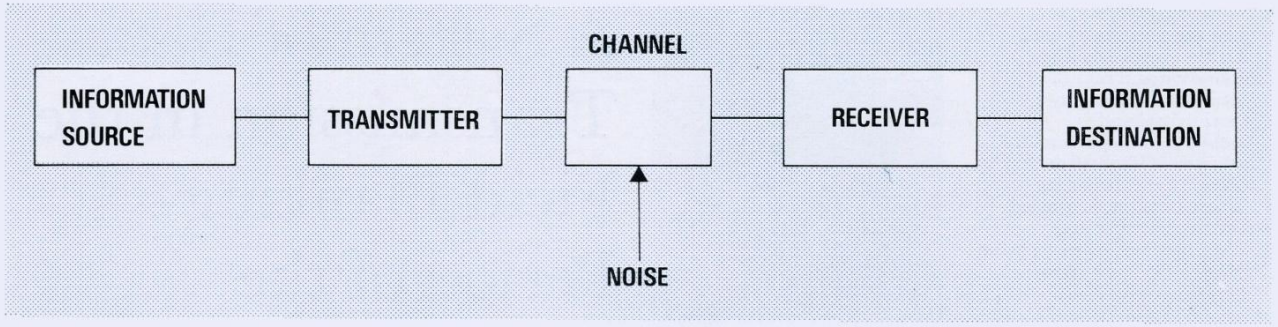


Fig.36. A typical data transmission system is shown. The channel or video distribution path is the part of the chain which imposes the overriding constraints on the system.

channel or video distribution path which places the overriding constraints on the performance, data capacity, and design of the transmission system. The data channel is represented in greater detail by Fig.37. The data channel is only available at times when the video switch allows transmission of data.

Synchronization and time availability

The video path is available during line 16, 329 at intervals of 20 ms. The duration of the data signal is a maximum of the active line time; this is defined[2] to be a minimum of 51·7 μs. Insertion data can thus be transmitted every 20 ms for a period of 51·7 μs. The ratio of 20 ms to 51·7 μs is so large that the data channel can be considered to be available 'intermittently' from the point of view of data synchronization. This infers that each line of data should be transmitted quite independently of previous messages.

A data receiver must not only derive a faithful replica of the transmitted wave shape, but must also be

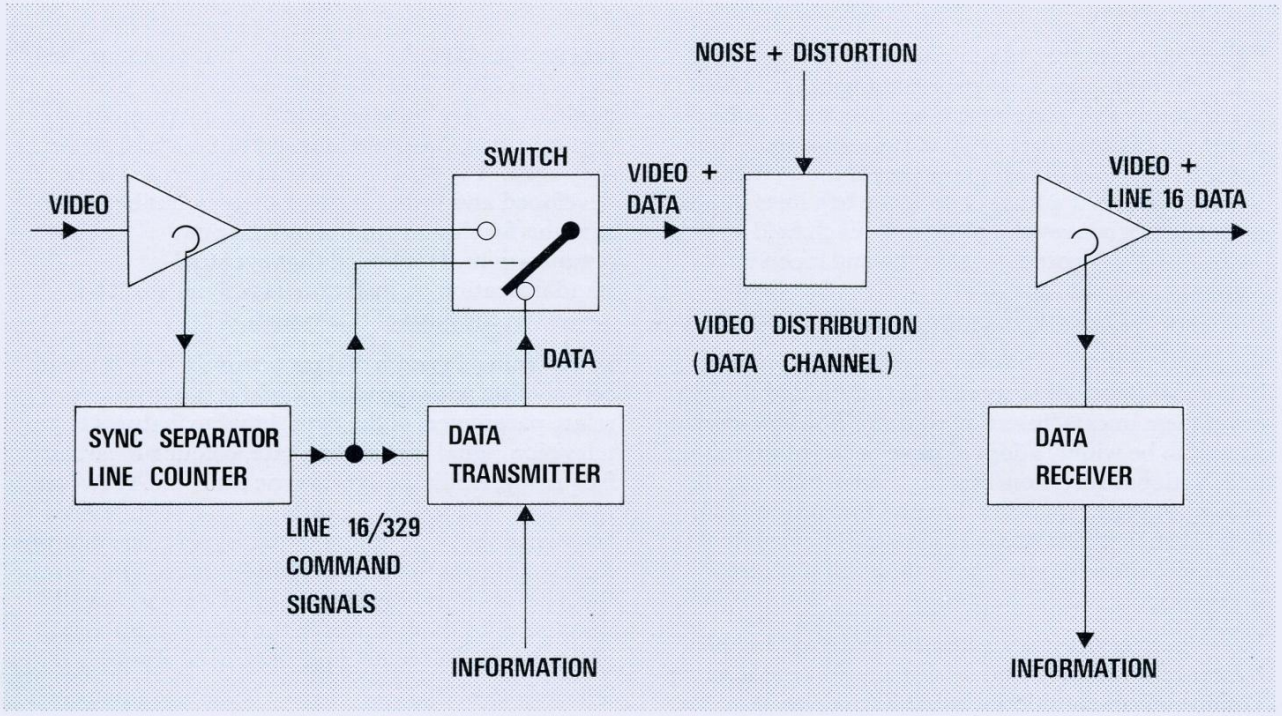


Fig.37. A more detailed diagram of the system shown in Fig.36 is given here. The data channel is only available at times when the video switch allows transmission of data.

provided with or derive from the signal a source of timing, the receiver clock, which allows the received signal to be sampled at the correct intervals. Only in this way can the information content of the signal be derived. In the case of insertion data the timing must be established at the beginning of each line 16. This defines the system as being partially coherent and the data must thus be prefaced with a timing bearing sequence. Once the timing has been established it may be allowed to free-run in an approximately optimum phase with respect to ideal sampling points, or it may be kept closely in phase by employing timing information derived from the signal itself, that is a self-timing system. A self-timing system is more rugged, allows easier insertion/extraction of groups of data and is thus favoured. The self timing feature must persist for all data sequences.

The data signal commences with the timing signal and in order to signify the commencement of data information a start sequence is necessary as soon as synchronization has been reliably established. Since the transmission time is short it is evident that both synchronization (run-in) and start sequence should be kept as short as possible to allow maximum time for information data transmission. Time considerations thus lead to the requirement for a partially coherent, self synchronizing, start-stop system of data transmission with minimum, but adequate length run-in and start code sequence.

Data signal power

The data signal is part of the video signal and it must obey the restrictions made on the video waveform. In particular the amplitude of the data signal must lie within the picture range of 0·3 to 1·0 V with respect to peak syncs. In this application it is thus peak power, or peak voltage, which is the limitation rather than the often considered average, rms power limitation. By using a signal of 0·7 V peak excursion, maximum performance in presence of noise will be achieved. No serious objection to the use of signals causing peak white on receivers or monitors, outside picture time, has yet been encountered.

Video frequency characteristic

The amplitude/frequency response of the video path is essentially flat from 0 to 5·5 MHz (5 MHz in Europe). The data signal must clearly contain frequencies restricted to this band. The phase/frequency response is ideally linear, i.e. the 2T pulse response should possess minimum lobes. This is the ideal condition for data transmission, and it is fortunate that both uses of the channel should require the same conditions. Quite contrary conditions apply in telephonic data transmission where the phase/frequency characteristic of the channel is almost immaterial for speech transmission. It is nevertheless very important that the data system should tolerate maximum possible deterioration from the ideal linear responses of the video channel. This infers that a two level data system should be selected rather than a multi-level system so that reflections and distortions will have minimum likelihood of crossing the zero-one signal level threshold.

Noise

Noise levels on the network are normally very low. As the signal passes through several RBR links noise increases but would not normally be worse than 35 dB pk signal/noise.

Effects of noise on the data become very important in applications such as monitoring of remote RBR transmitters at the main transmitter, or reception of data by outside broadcast vehicles for, say, gen-locking control in a marginal reception area. Further, if insertion data signals are to be used in conjunction with domestic receivers, where reception conditions can be very poor, a highly rugged system of data transmission is essential.

Independence of data from picture

The insertion of data depends on reliable access to the line 16 time slot. This is dependent on the sync separator which allows the line 16 positions to be sensed. Maximum performance of a sync separator is typically limited to 22 dB S/N ratio, and data cannot be inserted below this level.

The return off-air signal from an RBR transmitter could well have a S/N ratio of 0 dB. A data receiver should thus operate in noise levels which are as high as possible. To perform below 22 dB the reception must be independent of a sync separator. The data signal should be decoded reliably even though the receiver is exposed to a noisy video signal for 623/625 of the time, and the video signal should not cause the generation of a spurious received signal. Moreover, a data signal not requiring reference to video signal parameters allows the construction of a very simple decoder.

The modulation system

The various requirements of the insertion data system are:

a Good performance at poor S/N ratios.
b Timing component derivable from signal.
c Reasonably high information transfer rate.

d High security against incorrect message reception.
e Low likelihood of data signal generation from picture or noise.
f Signal spectrum well contained within channel bandwith.
g Simple equipment realization.
h Zero mean level variation, allowing capacitative data signal coupling.
i Easy insertion/extraction of parts of data signal at intermediate points.

The above requirements, together with the foregoing comments, lead very naturally to the choice of a data format which is described as partially coherent, self synchronizing, non-return-to-zero, complemented element transmission at a bit rate of 2·5 Mbits per second. The signal is illustrated in Fig.38.

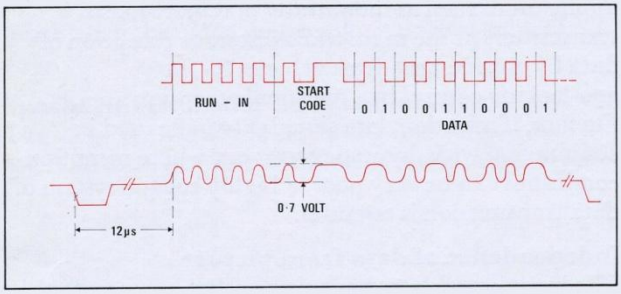


Fig.38. The data is shown here as a regular pulse train, and beneath as the filtered line signal. This signalling method may be termed 'binary partially coherent, self-synchronizing, non-return-to-zero, complemented element transmission'.

A 'one' bit is coded as a positive element of duration 200 ns, followed by a zero element. A zero bit is similarly coded as a zero followed by a positive element. The sequence of elements constitutes a polar binary non-return to zero code with the constraint that no more than two adjacent elements may have the same polarity. Transitions between zero and one thus occur at least every 400ns and it is these transitions which are used to generate the self-timing receive clock. The coded sequence is passed through a $\sin^2(t)$ shaping filter[3], a sequence of zeros thus appears as a 2·5 MHz sinewave at the modulator output. The modulation can be equally well described as 180° phase modulation, polar amplitude modulation, DSBSC amplitude modulation, of a 2·5 MHz carrier. It is most appropriate to think in terms of the complemented element description.

The run-in
Apart from a dc pedestal of 0·35 V, the signal has zero dc variation. It may thus be decoded after capacitative coupling. The dc component is lost during the start of the run-in, and during the latter part of the run-in transitions about 0 V are used to cause the receive clock to build up. Ten elements of run-in were found sufficient to synchronize the receiver reliably at 10 dB signal to noise ratio. Experiments were conducted using a phase locked loop for timing derivation, but a conventional tuned circuit using an inductor possessing a Q of approximately 80 at 5 MHz was found superior.

The start code
A start code of eight elements was selected. This is found to be sufficiently long to provide adequate security against chance generation (in combination with other security measures). The start sequence is made unique by including three adjacent '1' elements to prevent the data from generating a false start code. Additionally the mean level of the start code is 0·35 V in common with the data.

Field code
A two-bit field indication code was included in the data signal itself as a first level of information multiplexing in this first stage data system. It is then not necessary to examine the field sync signal to determine whether a line 16 or line 329 data signal is being received.

Information data
The maximum theoretically possible binary signalling rate in a 5 MHz channel is 10 Mbits per second. Employing realizable filters this rate is in practice reduced to 5 Mbits. An information rate of 2·5 Mbits was finally chosen as a reasonable compromise between maximum data rate and also satisfying all the other previously listed requirements. This allows 14 words of eight bits to be transmitted on line 16, not including the starting sequence. The capacity of line 16/329 is then 5600 bits per second, approximately twice the capacity of a good telephone line connection.

Signal filtering
For optimum performance in white gaussian noise, impulse signals are in theory transmitted through transmit and receive filters of cosine *f* form. Such an arrangement of filters has also near optimum effect against impulse noise.[4] The total channel characteristic would thus has a $\text{cosine}^2(f)$ form up to 5 MHz.

In practice the system concentrates filtering at the transmitter, so achieving a signal on line 16

possessing approximately sinusoidal shaped transitions. The shortest data pulse is 200 ns in width and thus corresponds to a 2T pulse shape. The receiver also incorporates a 5 MHz low pass noise suppression filter. The overall penalty in noise performance arising from non-ideal filtering renders no more than a 2 dB penalty in performance and is not serious.

Signal spectrum

Let us consider the mathematical form of these signals. Ignoring the dc pedestal, a single bit can be represented by the superposition of a pair of complementary 2T pulses above and below zero, separated by a time 2T.

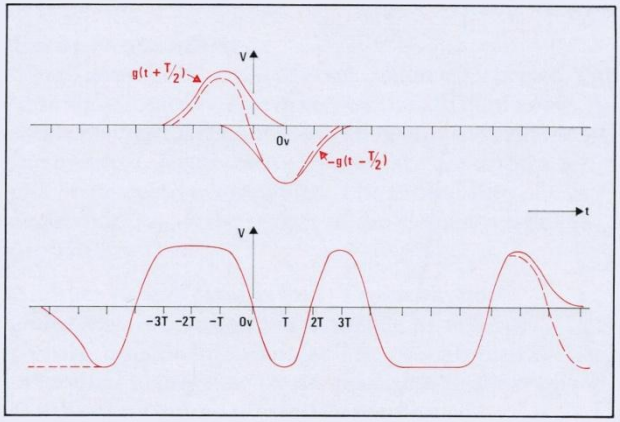


Fig.39. The structure of complemented element data is shown here. The whole data stream is constituted of pairs of complementary 2T pulses above and below zero separated by a time 2T. The real world signal only departs from that shown here at the extreme ends (where it must be at black level) and this is seen as a dotted line.

It can easily be seen how the whole data system is constituted of such pairs. The real word signal only departs from the representation in Fig.39 at the extreme ends (where it must be at black level) and this is seen as a dotted line. Apart from this negligible end effect the representation is precise.
The spectrum of the 2T pulse can be derived by standard Fourier mathematics, shown in Fig.40 as $G_1(f)$. The rule of superposition allows us to derive the spectrum of the complemented element signal by addition also in the frequency domain. The result, $G_2(f)$, is the spectrum of the complemented element pair. (In fact this is the formula for a 'one' bit rather than a zero.)

Normally to derive the **spectral energy density** of a random data train we require to derive the autocorrelation function of the signal. The Fourier transform of this function gives the power spectral density. However, in this case, because of the simple 180° phase relationship between 'zero' and 'one' bits, and the fact that the spectral density function contains no phase information, the spectral energy density function of the single bit is exactly the same shape as the power spectral density of a random sequence. So $P(f)$, the power spectral density, apart from a constant, is equal to the square of the modulus of the second equation $G_2(f)$. This function is shown in full on the bottom of Fig.40. The final practical result of these considerations is the graph (Fig.41) of the energy density of line 16 data which represents both single bit and random pulse train. It can be seen that the distribution is very well matched to the video channel. There is zero dc component and minimal energy below 100 kHz and

$$G_1(f) = 2T\left\{\text{sinc}(2fT) + \tfrac{1}{2}\,\text{sinc}\left[(f+\tfrac{1}{2T})2T\right] + \tfrac{1}{2}\,\text{sinc}\left[(f-\tfrac{1}{2T})2T\right]\right\}$$

$$G_2(f) = 2G_1(f)\sin(\pi fT)e^{j\pi/2}$$

$$P(f) = (2T)^2\,|G_2(f)|^2$$

$$P(f) = \left\{\text{sinc}(2fT) + \tfrac{1}{2}\,\text{sinc}\left[(f+\tfrac{1}{2T})2T\right] + \tfrac{1}{2}\,\text{sinc}\left[(f-\tfrac{1}{2T})2T\right]\right\}^2 \times \left\{\sin^2(\pi fT)\right\}$$

Fig.40. The spectrum of the 2T pulse can be derived by standard Fourier mathematics, shown here as $G_1(f)$. $G_2(f)$ is the spectrum of the complemented element pair; and $P(f)$, the power spectral density, is equal to the square of the modulus of $G_2(f)$.

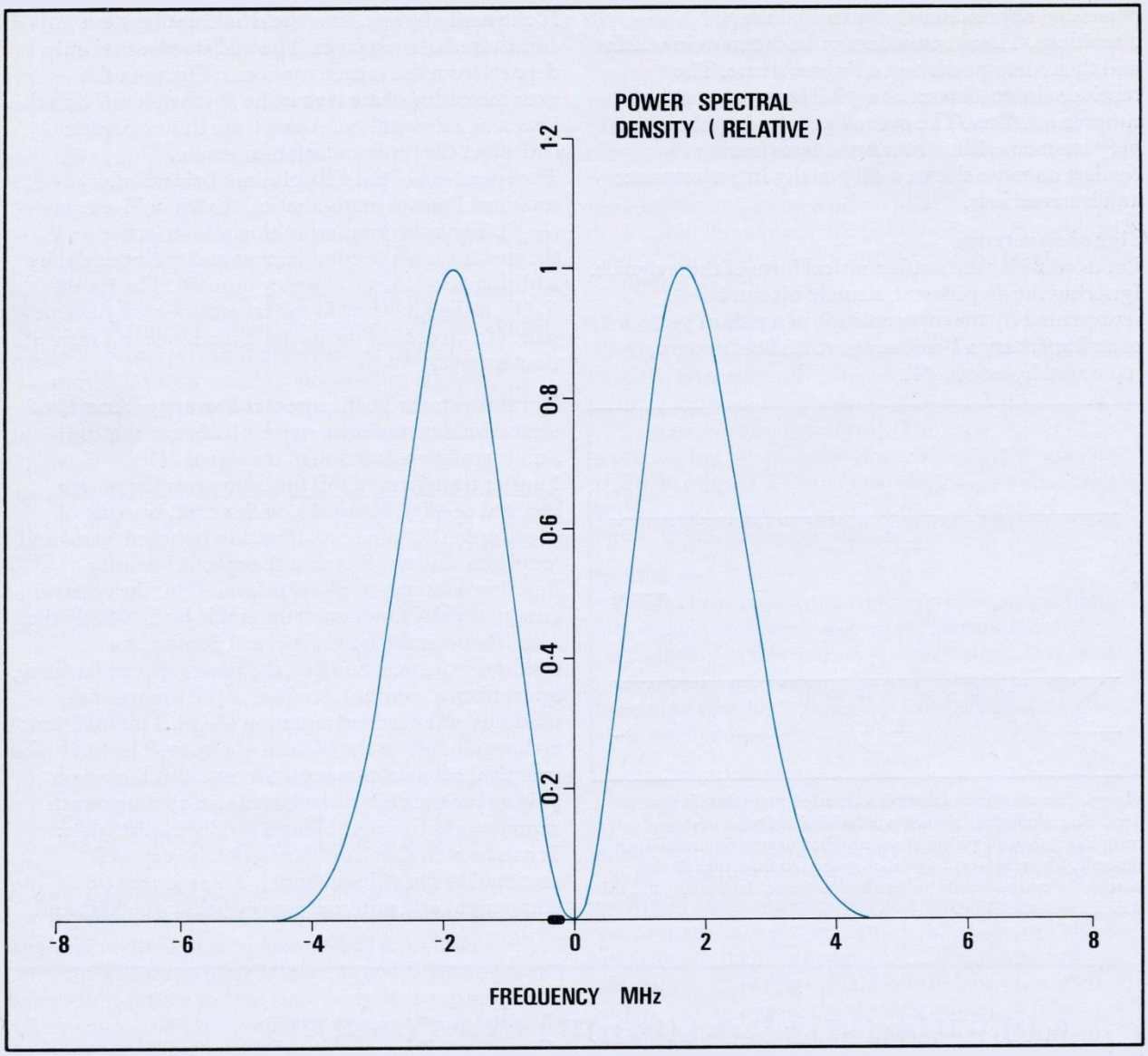


Fig.41. Above is a graph of the energy density of line 16 data which represents both single bit and random pulse train. There is a zero dc component and minimal energy below 100 kHz and above 4 MHz giving good protection from band edge distortions. The energy is more concentrated towards the band centre, and with even less energy above 5·0 MHz than the 2T pulse, by virtue of the complementation.

above 4 MHz, giving good protection from band edge distortions. The energy is in fact more concentrated toward the band centre, and with even less energy above 5 MHz than the 2T pulse, by virtue of the complementation. Above 5 MHz the energy just manages to shift the computer incremental plotter by one increment.

Timing

Impulses derived from the zero crossings of the ac coupled data signal are used to energize the clock-tank circuit. An additional feature is incorporated in the receiver, the clock level detector, so that only when the clock oscillations are above a certain threshold is the clock signal accepted as

valid and the data accepted. This effects an increased security against data generation by picture of noise.

Data receiver

Element by element detection of the data signal is employed. A receiver is simply illustrated in Fig.42. Before accepting the data signal as valid, the complete start code is accepted, all bits are checked for element parity, the clock tank signal must pass its amplitude threshold, and as a further security a simple window triggered by a simple field sync detector can be employed to prevent the very remote chance of picture generating a valid data signal. The output signal from the receiver is a multiple output from data latches which changes when a new word is received on line 16.

Error probabilities

There are several types of error which may occur. The data signal may be corrupted by the effect of noise. A single element wrongly received results in rejection of the message. If adjacent elements are distorted a bit can be detected erroneously. The probability of this occurring, Pe_B, is the square of the element error probability Pe_E.

Another type of error is that of coincidental generation of a valid data sequence by noise or picture, outside line 16 data. The probability can be prevented in any case by the provision in the receiver of the data window previously mentioned.

The theoretical performance of complemented element coding in noise is:

$P(eE)$	$P(eB)$	*S/N Ratio (dB)*
10^{-2}	10^{-4}	12
10^{-3}	10^{-6}	15
10^{-4}	10^{-8}	16
10^{-5}	10^{-10}	18
10^{-7}	10^{-14}	20

The S/N ratio is peak (0·7 V) signal to rms noise.

Tests

The system of data transmission has been implemented and tested: The following table shows the performance in noise.

Pe_E	Pe_B	*S/N ratio observed (dB)*	*Theoretical (dB)*
5×10^{-2}	25×10^{-4}	10·8	—
10^{-2}	10^{-4}	12·8	12
10^{-3}	10^{-6}	15·3	15
10^{-4}	10	16·8	16·4

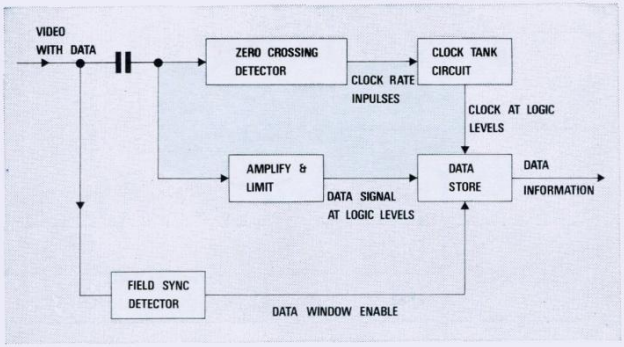


Fig.42. A data receiver is shown. Before accepting the data signal as valid, the complete start code is accepted and all bits are checked for element parity. A window triggered by a field sync detector is used to prevent the very remote chance of picture generating a valid data signal.

Degradations in noise tolerable for a constant error rate have been observed on the network, over air under different conditions of reception and in the presence of distortions produced in the laboratory. These results are:

Conditions of test	*S/N ratio for* 10^{-3} *PeE (dB)*	*Reduction in performance (dB)*
Theoretical performance	15·0	—
Local direct connection	15·4	0·4
IBA E133 receiver off-air	17·4	2·4
Commercial receiver off-air with poor quality aerial system	22·0	7·0
20% white crushing	18·0	4·0
Phase distortion producing 30% 2T pulse undershoot	26·0	12·0

Programme source identification

The first application of the data system at the IBA is for labelling programme sources within the IBA programme network. The data signal is inserted along with insertion test signals (ITS) on the adjacent lines 19, 20, 332, 333, and the data signal when read out and displayed on an indicator denotes the sources of ITS and also programme. The system is currently demonstrating a solution to live programme identification and providing an extended test of the data system under operational conditions. No severe problems have yet been encountered. Some further possible uses of insertion data are:

Source identification.
Programme category.
Destination of transmission.
Quality rating of original signal.

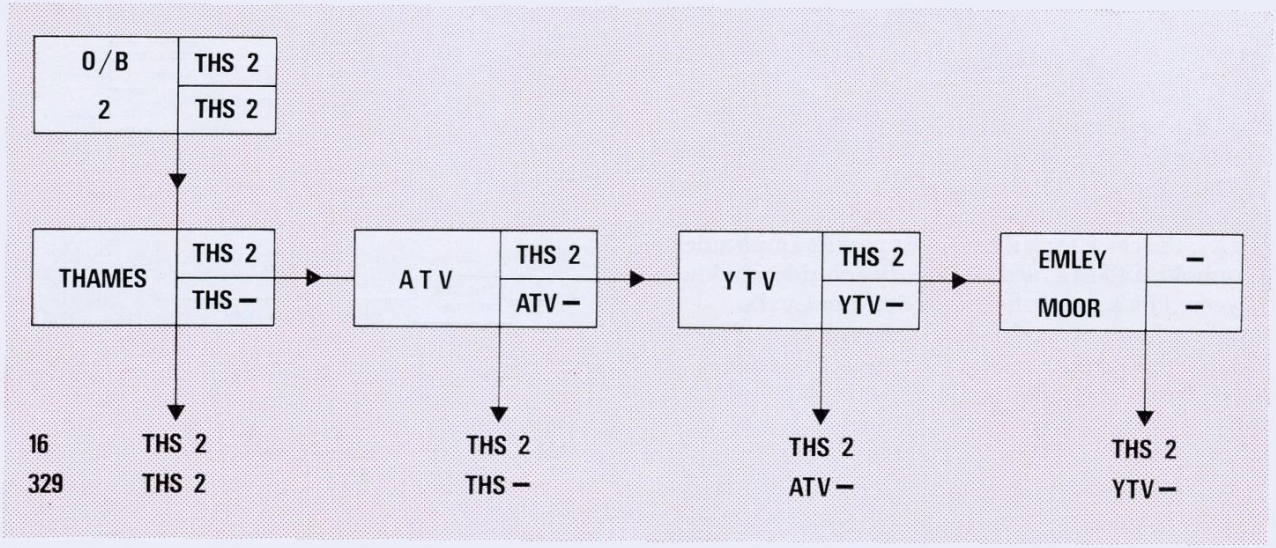


Fig.43. The diagram shows how the SLICE system works. Line 16 carries the originating source label, in this case Thames (THS) OB No. 2, and this remains together with the associated test lines on lines 19, 20, throughout the system up to the transmitter. Line 329, on the other hand, is re-labelled at each routing point, together with the associated test lines on 332, 333. At the bottom is displayed the readout of information obtained at each point.

Switching and routing instructions.
Source synchronization, OB genlock.
Monitoring and service data.
Telemetry to remote transmitters.
Programme co-ordination.
VTR frame numbering.
Network time signal.
Transmission of captions to special domestic receivers.
Transmission of instructions and information to subsidiary studios, transmitters, displayed on monitors or print-outs.
Communication with OB units.
Message transmission for ETV distribution, selective user addressing.
Verification of carriage of commercial material, using line 16 monitoring.
Remote control of unattended VTRs.
Regional news and/or weather service distribution.
Domestic information service as with the proposed 'Oracle' service *(see page 61)*.

Conclusion

The development of a system of data transmission using insertion data signals on line 16 has been brought to the point where a first-stage system is being put in the field for the application of live programme source labelling.
To take advantage of the full potential of insertion data the application and allocation of this data channel must be carefully planned and controlled. Studies are proceeding at the IBA to develop a system of multiplexing equipment which will render maximum user benefit of the available data channel and allow the many possible uses to be put simply into practice.

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4. W R Bennett, and J R Davey, *Data Transmission*, McGraw Hill, 1965.

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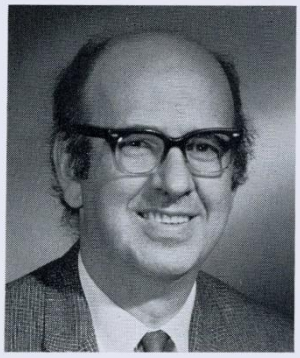


The Digital Future of Television Studio Centres

by J L E Baldwin

Synopsis

When digital techniques are adopted for a signal path considerable benefit is obtained: providing the characteristics of that path are sufficient to permit correct identification of the states of the signal, then no degradation will occur, the overall result being indistinguishable from that obtained with an ideal path.

For this reason, this article initially assumes that the technique adopted for video processing and distribution in a studio centre should be exclusively digital. In practice, the earliest point at which conversion to a digital format can be achieved is immediately after the head amplifier in the camera.

The various parts of a possible digital chain are considered including cameras, coders, mixers, videotape recorders, and monitoring equipment. Particular attention is given to the realization of digital videotape recorders and PAL coders.

A comparison of projected relative costs for studio centres using analogue and digital equipment indicates that the latter would be more expensive at present but that the break-even point might occur as soon as 1976.

Although digital techniques are only now beginning to replace conventional methods in a wide range of technology, they are in many ways more basic and obvious.

Much of nature itself is digital. All matter is composed of fundamental and discrete particles and so one could argue, for example, that mass is a digital quantity; the mass of an object can only increase by certain fixed values, albeit very small ones. Light is also digital, if by digital we mean that it comes in 'packets' with the energy contained in each 'packet' being directly proportional to the frequency. Even an analogue electrical signal could be said to be digital since it varies only in finite increments of charge, the unit increment being the charge on a single electron.

In exploring, therefore, the use of digital techniques, with all their attendant advantages of stability, ruggedness and 'go–no go' characteristics, we are not really dealing with a brand new concept but rather modifying and adapting something completely natural. Of course, with present technology, the idea of counting individual electrons is beyond the realms of possibility; if the signal current from the 'red' tube of a Plumbicon-type camera is 0·1 μA in the picture highlights, the number of electrons delivered from the tube in precisely 75 ns (this would be an appropriate time for a television system having a signal bandwidth of 5 MHz) would be 46,800. This example does, however, illustrate a digital process, and indeed the transformation that occurs in an analogue-to-digital converter. The output from such a converter is always a whole number representing in mathematical form the magnitude of the input signal or some function of it.

We shall now see how digital methods and principles might be applied specifically to television studio equipment and may replace the conventional, less satisfactory analogue systems now in use.

Camera

In digital practice, it is usual to express an output number or quantity in binary form and in practical terms, for a normal gamma-corrected, composite, PAL-encoded video signal a binary number or word of eight bits is generally adequate. An extra one or

two bits would be needed due to the greater gain provided by the gamma-corrector in the darker portions of the picture. However, at this point in a camera it is unnecessary to handle the synchronizing pulses or coded chrominance signals; so one additional bit should be sufficient, making the required word size nine bits.

For a practical camera, as we have said, it is impossible to count the electrons from the camera tube, and so it is necessary to use a conventional head amplifier followed immediately by an analogue-to-digital converter.
The fundamental operations that have to take place in the video chain of a colour camera are:

1. Establishing black level.
2. Halation correction.

3a. For 'live' cameras – colour matrixing to improve colour rendition.

3b. For telecine cameras – colour masking to compensate for the film dye characteristics.

4. Gamma correction.
5. Aperture correction, both horizontal and vertical.
6. Blanking.
7. Cancellation of any bias light.
8. Colour balancing.
9. Peak clipping.

There can be little doubt that each of these operations could now be realized in digital form; but the cost and size of the resulting equipment would be excessive. A major part of the total cost would be three analogue-to-digital converters. Soon, however, it may be possible for each a–d converter to be formed on a few chips, costing about £20 (USA $50). Clearly it is not possible to forecast exactly when such integrated-circuit converters will be available, but it seems virtually certain that this will happen.

One great advantage resulting from the use of digital techniques in the video chains of such a camera would be that the digital chain itself would not drift and would have no preset controls; indeed each video chain would be working just as a calculator, operating on numbers.

Colour encoding

It is assumed that the radiated television signal will remain – at least for many years – in its present analogue form with colour information encoded in the PAL system. The realization of a coder capable of producing such signals directly in digital form is described below; the modifications which would be required for an NTSC signal will be self-evident; SECAM, on the other hand, would need a different approach.

Provided that the input signals to the coder are sampled at the third (or higher) harmonic of the subcarrier frequency then the coding operation can be realized in a fairly straightforward manner. In general, the steps in this operation are directly equivalent to those used in an analogue converter and will follow the same sequence.

It is assumed that the camera provides three digitally-coded outputs, representing the red, green, and blue components of the signal. It is further assumed that these outputs have black level corresponding to one specific number, with peak white level corresponding to another specific number, and that each signal has been sampled at precisely three times the colour subcarrier frequency.

A way of achieving the coding of these signals would be to use the following six steps in sequence:

1. Obtain the luminance number by adding together appropriate proportions of the numbers representing the three colour signals.
2. Produce R–Y and B–Y signals by subtracting the luminance number from the numbers representing the red and blue signals. Since the answer may be positive or negative a suitable numbering system must be adopted. Inevitably, the number representing zero colour will itself be zero.
3. Gate in an appropriate number to each of the R–Y and B–Y signals during the required burst gate time, and gate in zero during the remainder of the blanking time. These will eventually yield a shaped burst waveform and will remove unwanted chrominance noise during blanking.
4. Pass the R–Y and B–Y signals through digital filters to control the chrominance frequency response and (incidentally) the shape of the burst. Appropriate scaling factors would be incorporated, including a factor of $\sqrt{\frac{3}{4}}$ for R–Y.
5. Delay the luminance path by a specific number of 'words' to compensate for the delay in the digital filters, and add the sync pulse information.
6. Assemble the signal by adding the luminance and filtered and scaled colour-difference 'words', in accordance with the following repetitive sequence:
   a Y + (B – Y)
   b Y – ½ (B – Y) + (R–Y)
   c Y – ½ (B – Y) – (R–Y)
   for lines with the burst of 135°. For the intermediate lines, with the burst at 225°, the repeating sequence would be *a*, *c*, *b*, and so on.

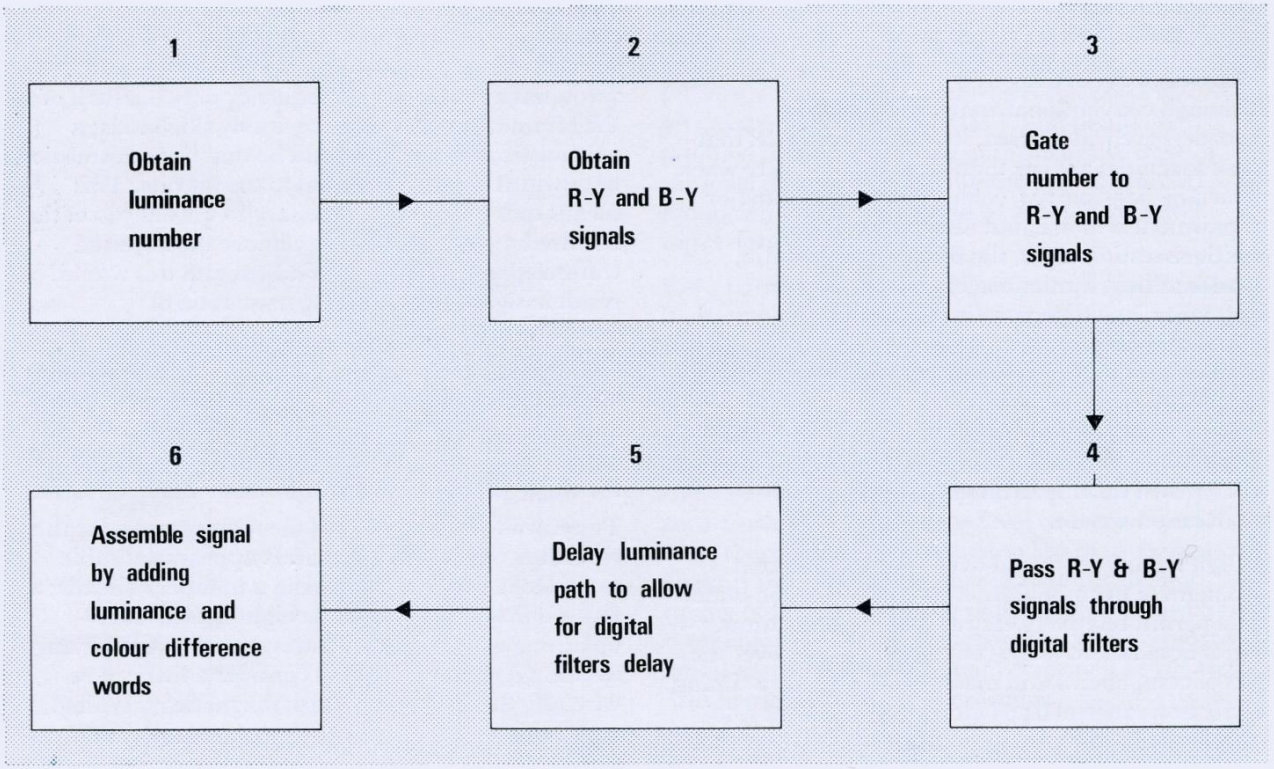


Fig.44. One method is shown of encoding the three digitally-coded outputs from a camera. It is assumed that the outputs have black level corresponding to one specific number, with peak white level corresponding to another number, and that each signal has been sampled at precisely three times the colour subcarrier frequency.

The relatively simple formulae indicated above result from using a sampling frequency precisely three times subcarrier frequency and by selecting an advantageous phase relationship. Not only does this phase relationship make the equipment design easier, but it also gives the significant additional advantage that all signals will be either in correct phase or displaced by plus or minus 120°; correct phasing can always be obtained by advancing or delaying the whole signal by one word.
The advantages of such a digital colour coder would include the complete absence of drift and the elimination of all setting up controls.

Mixing

If all the signals were digital, then – with the type of encoding described above – the problems of colour phasing would be minimal and could easily be made automatic.

Automatic synchronization of the line timing and the phase alternation would be relatively easy, but automatic field synchronization would be more difficult and expensive to implement. The cost of the storage elements for a field of storage is now about £3000 for 525-line operation and £4500 for 625 lines. Since mixing is a simple arithmetic operation, it will not be described in detail.

Monitoring

In present practice, the quality of the transmitted signals must be monitored at various points along the transmission chain. Basically, monitoring serves two purposes. The first is to ascertain whether the picture is artistically correct and the second is to discover whether there are any technical errors.

To make monitoring reasonably economical it would be necessary to have low-cost digital-to-analogue converters. In the long term it would be even better to have direct digital-to-RGB decoders.

It must also be remembered that with a digital system impairments, such as noise, chrominance/luminance delay or gain inequalities, smearing, differential gain, and so on will not exist. Provided that the ones and

zeros have been correctly identified, no errors can be introduced into a digital system.

Videotape recording

Although conventional analogue videotape recorders are widely used, it must be admitted that these machines are less than ideal, particularly when recording 625-line PAL colour pictures. The major impairment is moiré; but also, with normal multigeneration tapes, the signal-to-noise ratio, head-banding, luminance/chrominance gain inequality, line time non-linearity, and differential gain may all, quite often, cause significant impairments to the picture. A digital recorder would not produce such errors.

Present analogue recorders are expensive because of the required long-term timing accuracy (about 1–2 ns). Most of the impairments result from the modulation system.

A digital recorder would overcome the inherent problems of the modulation system and at the same time permit relatively easy and economical timing correction. About £150 (USA $400) would cover the cost of components and materials to provide a timing correction range of 64 μs increasing by about £50 (USA $130) for each additional 64 μs. Clearly such timing correction would be much cheaper than that used with current analogue machines, even if it has sufficient range to compensate for the larger timing errors that might be expected from the use of simpler and cheaper tape transports and servo systems.

Realization of a digital television recorder

The required bit rate for a 625-line television signal using eight bits per word is about 106 Megabits per second. At first sight, it might appear difficult to achieve such a high bit-rate of recording. But it is worth asking whether this view is valid – indeed, the following argument suggests that it may well not be: Suppose that between a transmitting point and a receiving point there are 100 video cables, each having identical delay and equalized to 5·5 MHz. Suppose that unfortunately the cables are very noisy, having peak signal-to-rms noise ratios of only 20 dB, and that the noise on the different paths is uncorrelated. By passing the same signal along all the cables adding the outputs, the signal voltages would add and similarly the noise power: this would yield a resultant signal-to-noise ratio of 40 dB peak signal to rms noise. This would represent a performance comparable with that of an analogue videotape recorder.

On the other hand, each path represents an adequate signal-to-noise ratio for the transmission of a binary signal. A binary signal, with alternating ones and zeros, has a fundamental frequency only one-half of the bit rate, but there are inevitably sidebands; a pessimistic assumption would be that the transmission bandwidth needs to be equal to the bit rate. This means that it would be necessary to use only 20 of the hundred 5·5 MHz cables to achieve the required transmission capacity of 106 Mb/s, and this would result in signal to quantizing noise ratio of (theoretically) 58·8 dB.

This indicates that in this particular case, by opting for a digital signal, it becomes possible to transmit along the 100 cables five programmes, each with a better signal-to-noise ratio than could be obtained for the single programme transmitted in analogue form.

To return to the question of the requirements for the recording of a 625-line signal. It appears desirable to divide the data rate between a number of heads; a natural first choice would be eight heads, each operating at 13·3 Mb/s. However, before taking any decision it would be wise to consider a little more carefully the characteristics of magnetic recording.

Factors which need to be considered include:

1. The minimum wavelength that can be reproduced satisfactorily is about 100 μ in. (2·54 μm).
2. Drop-outs occur, often caused by surface irregularities or dust particles; a drop of 54·6 dB occurs per wavelength separation of the head pole-tips from the magnetic coating.
3. Variations of signal level result from changes in the pressure between head and tape.
4. The signal level is modulated by electrical or magnetic variations in the coupling between the stationary deck and the rotating heads.
5. The magnetic characteristics of tape vary along its length and from sample to sample.
6. Tape has non-linear magnetic characteristics.

Items 2–5 all result in amplitude modulation, and this can be further aggravated by item 6. It follows, therefore, that any form of amplitude modulation of the signal is likely to fail and that a better method is to consider only the sign of the signal and to ignore its magnitude. It might appear, at first sight, that only a single binary signal could be handled by each head – however, this is not strictly true since it is possible to consider the times at which the signal changes sign, assuming that a 'clock' can be provided. This technique may well be considered as a form of phase modulation.

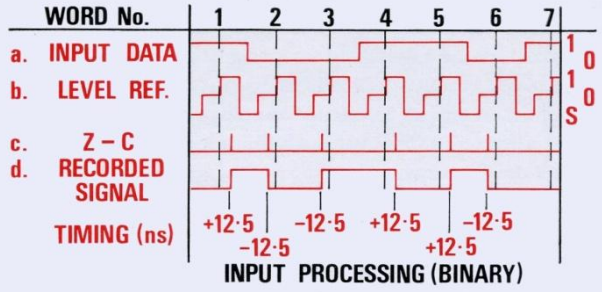


Fig.45a. This shows a form of binary coding which would be suitable for recording a PAL 625-line signal. When identity occurs between the states of the input data (a) and the level reference (b) a pulse (c) is produced which changes the sign of the recorded signal (d), as shown in the fourth line.

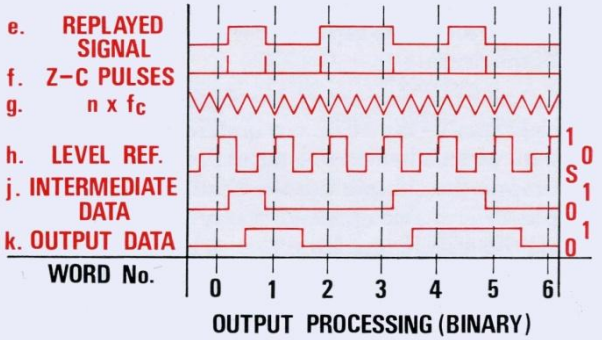


Fig.45b. The replay process is illustrated. The replayed signal (e) from the tape is shown in idealized form. The signal is differentiated and full-wave rectified, so providing a zero-crossing pulse (f) whenever a change of sign occurs. These pulses are used to energize a resonant circuit at a multiple of the required clock frequency, and this can readily be divided to yield the reply level reference (h). The zero-crossing pulses are used to sample the level reference (h) giving the intermediate date (j) and finally this is sampled just after the time of the negative edge of the level reference (h) giving the output data signal (k), which is identical to the input data (a).

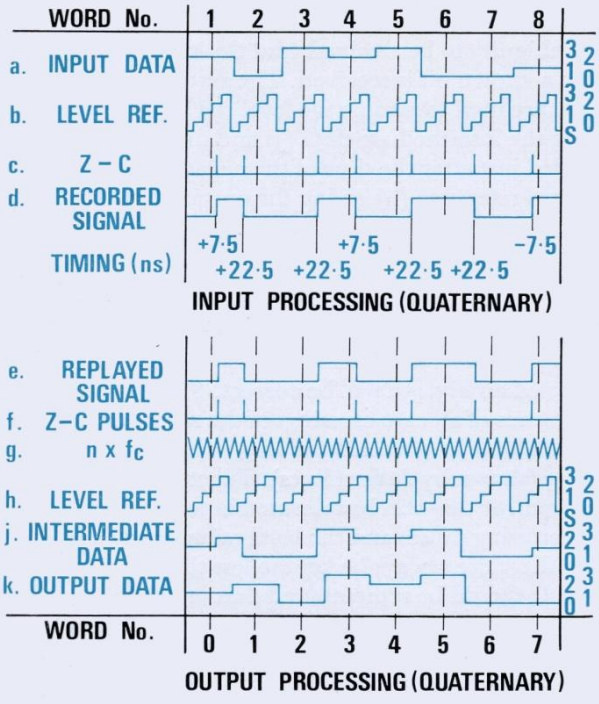
A form of binary coding offering useful advantages is shown in Fig.45a. The input data (a) is shown at the top. When identity occurs between the states of the input data (a) and the level reference (b) – shown on the next line – a pulse is produced (c) which changes the sign of the recorded signal (d) as shown in the fourth line. The replayed signal (e) from the tape is shown in idealized form at the top of Fig.45b which outlines the replay processing. The signal is differentiated and full-wave rectified, so providing a zero-crossing pulse (f) whenever a change of sign occurs. These pulses are used to energize a resonant circuit at a multiple of the required clock frequency, and this can readily be divided to yield the replay level reference (h) shown on the fourth line. There remains an ambiguity to be resolved, and this can be done when a known bit is received. The zero-crossing pulses are used to sample the level reference (h) giving the intermediate data (j) and finally this is sampled just after the time of the negative edge of the level reference (h) giving the output data (k) signal, which will be seen to be a duplicate of the input data (a) of Fig.45a.

For a 625-line video signal the appropriate duration for each word is just over 75 ns, so that, assuming that one bit per word is recorded on each track, the times indicated on Fig.45a will be correct. The time of occurrence of all zero crossings of the recorded signal will be either 12·5 ns early or 12·5 ns late on the mean timing (shown by dashed lines). The maximum timing error that can be tolerated between the zero-crossing pulses and the level reference signal must therefore always be kept to less than 12·5 ns peak. It should be remembered that any drift of timing of the zero-crossing pulses will be followed by compensating timing changes of the level reference signal so that the predominant error will be the fast drift of timing of the zero-crossings.

Measurements indicate that such fast changes of timing are likely to amount to only 0·5 ns peak; there is thus a safety margin of about 25:1. The conditions under which these measurements were made were a head-to-tape speed of 1 500 in./sec. (38·1 m/sec.) and a track width of 0·01 in. (0·254 mm.).

It has been assumed so far that there is binary coding on each track, but there is no reason why quaternary or octal codes should not be considered.

Figures 46a and b illustrate the signals that arise for a quaternary code. The explanation already given in respect of Figs. 45a and b is equally relevant to this case and will not be repeated. The only significant difference is the use made of the redundancy which exists in the system; this is used whenever a zero immediately follows a three, but not the converse. When this condition arises, the zero-crossing is omitted (pulse *P*). This is identified during replay by the absence of any zero crossing through a complete cycle of the level reference (h); the zero is then reinserted. It would be dangerous to use this technique for all zeros, since a long string of them would result in the level reference signal becoming unlocked. However, by making use of this redundancy in the signal the duration of the



Figs.46a and b. A similar signal to that in Figs.45a and b system is illustrated using a quaternary code. This system makes use of the redundancy which exists in the system. When a zero immediately follows a three the zero-crossing is omitted (pulse *P*); this is identified during replay by the absence of any zero-crossing through a complete cycle of the level reference (h); the zero is then re-inserted. The duration of the minimum 'half' cycle of the recorded signal can be increased by 50% and this allows the adoption of a head-to-tape speed of only two-thirds of what would otherwise be necessary.

minimum half cycle of the recorded signal can be increased by 50%; this may permit the adoption of a head-to-tape speed of only two-thirds of what would otherwise be necessary.

For this particular quaternary system, using a scale of four, a timing accuracy of better than 7·5 ns is required. If the track width be reduced from 0·01 to 0·0025 in., it is possible that the timing error could increase by a factor of 2:1, but this would still be less than about 1 ns peak.

With this narrow track width, it would appear practical to use an octal system, that is a scale of eight, and this would probably require a timing accuracy of better than 3·125 ns. Even this would yield a safety margin of 3:1 and this would appear adequate.

It is highly desirable that protection should be provided against drop-outs. An effective technique would be to use several parity bits in order to protect the more significant bits of each digital word, although it would also be essential to arrange that the probability of simultaneous drop-outs of information is low; for example to ensure that two heads would not be affected simultaneously by a longitudinal scratch on the tape.

A good system would be to have four heads in use at any time, each handling three bits; these would represent one of the four more significant bits; one of the four less significant bits; and a parity bit. The parity bits would be used together to correct or conceal errors occurring on the more significant bits recorded by the other heads.

Such a recorder might well be of the helical-scan type and have five video heads spaced at 72°. The extra head would allow the tape to be wrapped around only 288° of the drum.

To minimize tracking errors, the drum would be relatively small – say 10 in. circumference – and the tape 2 in. wide. The head-to-tape speed would be 1 250 in./sec.; to achieve this the head disc would rotate at 125 rev./sec., that is 7 500 rev./min. At 1 250 in./sec., the wavelength would be 188 μin. (4·75 μm) and the minimum half cycle a length of 47 μin. (1·19 μm). At a tape velocity of 15 in./sec., the centre-to-centre spacing of the tracks would be 0·0048 in. (0·123 mm), the track width 0·003 in. (0·0762 mm), giving a guard band of 0·0018 in. (0·0457 mm). This guard band is considered adequate for a 2-in. tape having a length of 8 in. of tape in contact with the drum.

While it may seem strange to consider using an analogue sound track on a digital video recorder, this would not detract from performance provided that the analogue system were adequate. Unfortunately, the dynamic range of conventional analogue systems is not sufficient – and all too often noise and distortion are apparent at the same time. Further, this problem is made much worse by the need to edit tapes together. Obviously a digital solution could be adopted.

Standards conversion

The cost of MOS shift registers is now down to about 0·25p per bit which may perhaps be better expressed as 400 bits/£ (154 bits/$). The speed of operation of such registers is still going up; some are usable at 10 Mb/sec. Converters and synchronizers both need significant storage capacity, and it is clear that the cheapest way to provide this is by the use of shift registers.

A digital line standards converter 1,2 (*see page 15*) was demonstrated to members of the Technical Committee of the European Broadcasting Union in March 1971; subsequently this experimental converter was used operationally for a period during the summer of 1971 to provide the 405-line signals for the IBA Croydon transmitter – the transmitter which serves the entire London region.

A digital field-rate standard converter (*see page 31*) has since been developed in the laboratories of the Authority's Experimental and Development Department; this converter produces noticeably less impairment than current analogue-type converters.

The future of digital television

In an era of direct satellite broadcasting and the 'wired city', it may well happen that domestic receivers will receive signals in digital form; however, it is not anticipated that this is likely to have significant practical impact before about 1990.

On the other hand, it is believed that studio complexes based on the use of digital techniques would be possible *now* – although clearly just when digital techniques are adopted widely will depend primarily on how the system cost compares with conventional analogue equipments.

However, as the cost of integrated circuits is steadily falling and cost-savings still to be expected from the exploitation of medium and large scale integration could be substantial, it could well be that by 1976 the cost of a digital studio complex would be less than its analogue equivalent. Whether, in fact, it will be possible by 1976 to assemble such a complex depends on when manufacturers start developing the component parts.

Obviously it will be difficult, and undesirable, to introduce digital equipment in a piecemeal way; but it appears possible to effect the change in a series of stages, preferably working backwards from the output of the studio complex toward the origination units in the studios. The timing of such radical changes must clearly depend on availability of equipment and on the need to re-equip existing studio centres or provide new ones.

But above all one question must be dominant: what will be the form of the digital 'video' signal? Without standardization, the problems of interfacing would be immense, if not insoluble.

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1. J L E Baldwin, 'New Techniques in Television Standards Conversion', *IBC 1970 Conference Publication No. 69*, pp.198–200.

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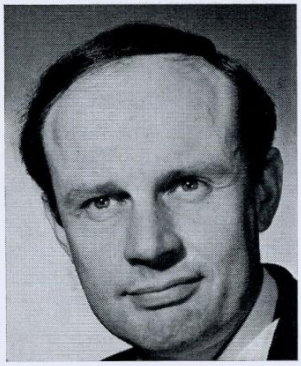


The Application of Digital Techniques to Radio Frequency Circuits

by F H Wise

Synopsis
The article shows how digital circuits, with all their advantages over traditional analogue techniques, may be used in transmitting and receiving equipment for such functions as modulation, demodulation, vestigial sideband filtering, group delay, and linearity correction, and includes a physical explanation of the various processes.

Broadcasters and manufacturers have invested considerable effort in the design of high-quality receiving and transmitting equipment and in most respects present designs are thought to provide a performance which is adequate for existing broadcasting systems. It would seem that greatest benefit would come from an improvement in maintainability. This is taken to imply better reliability, reduction in the number and complexity of adjustments needed in meeting a given standard of performance, and a reduction in the cost of stocks of spare parts. There is little doubt that digital methods would provide these advantages.

Below are considered the ways in which these techniques may be applied to rf circuit functions, the different design concepts needed, and the improved performance obtainable as compared with present designs. Circuit functions covered include those of modulation, demodulation, frequency synthesis, filtering, delay equilization and linearity correction. They are applicable both in the design of receivers and of transmitters used for various purposes, but this paper concentrates on television applications. Details of circuit design are not included.

Frequency synthesis

High-quality television waveform measuring receivers and test transmitters have to date been restricted to single-frequency operation. Change of channel has generally meant the substitution of a relatively expensive plug-in module, or the need for some complex realignment. One of the design problems contributing to this difficulty has been the need to provide oscillators with a different frequency for each channel but in each case controlled to a tolerance within $\pm 0{\cdot}001\%$.

This problem has now been solved by the use of digital synthesizers. A design produced by the IBA provides a choice of frequency in 8 MHz increments over the frequency range 500–900 MHz. A voltage controlled oscillator capable of being tuned over the required frequency range provides the output signal. Part of this VCO output is heterodyned into the frequency range 100–500 MHz where its frequency may be divided using presently available high-speed emitter coupled logic digital circuits having an operating capability up to 650 MHz. The division ratio is fixed at 16, so that for 8 MHz increments in VCO frequency, the output frequency of the high-speed divider changes by 0·5 MHz steps over the range 6·25–31·25 MHz. This signal is then applied to a divider which uses Schottky TTL and which can be programmed using a six-bit code to divide by any integer from 2 to 64 for input frequencies up to 40 MHz. The output from this variable divider is compared in a phase sensitive detector with that from a 0·5 MHz reference crystal oscillator. Any error signal from the PSD is used to control the VCO and thus to stabilize the output frequency which may be switched, in 8 MHz steps over the frequency range. If different offsets are needed, these may be introduced at the heterodyne oscillator used to change frequency immediately prior to counting.

As well as providing an operationally more convenient equipment, the availability of tunable equipment considerably eases stores holding problems. At present day costs, the break-even point for provision of a synthesizer as compared with separate oscillators occurs when operation is needed on five different channels.

Receivers

Before any detailed design may be commenced, the basic block diagram, intermediate frequency, and sample rate must be fixed. The requirement is for an A:D converter operating at the receiver IF followed by a filter network and a detector circuit. The output should be in a form compatible with existing standards, i.e. eight bits at a data rate of 13·3 MHz (three times subcarrier frequency).[1]

The restrictions in choice of IF differ as between analogue and digital systems. In designs intended for operation at many different signal frequencies, it is not normally possible for the designer to choose an IF which does not have a harmonic falling within the input passband. Analogue designs, therefore, have provision for the decoupling of these harmonics from receiver input circuits. Where the IF signal exists only in digitally coded form, the possibility of direct generation of IF harmonics cannot occur. Instead, the problem is exchanged for that of decoupling harmonics and subharmonics of the sample pulse repetition frequency which, in the design described in this paper, is at four times the IF carrier. In practice the problems are not greatly different.

There is one area where the use of digital IF circuits gives the designer complete freedom. This is in the removal of any restriction in the relationship between video and IF passbands. In analogue designs it is important that the two passbands do not overlap and normally it is necessary to provide some guard band. This arises because detector circuits cannot provide adequate isolation between input and output terminals. Where the detection is performed digitally, i.e. by application of some logic process, the train of data is merely being recoded and the problem of interaction does not arise.

Because the form of the output has been defined, it is necessary to start the consideration of system parameters at the detector.

Detector

The output sample rate is to be 13·3 MHz and the detection process required is that of 'synchronous' detection. This process[2,3] is normally realized in analogue systems by use of a circuit in which the IF signal is multiplied by a continuous wave oscillation, phase locked to the carrier. This allows the wanted (inphase) information to be recovered from an asymmetric sideband signal whilst excluding the unwanted (quadrature) information. Another way of considering the process, and one which may be more readily understood in the digital domain, is to visualize samples being taken at the peaks of the wanted component of the IF signal. If these samples are located accurately on the peaks of the inphase component, they are automatically located at the zeros of the quadrature component. Thus, a digital synchronous detection process may be formulated. It is necessary that the samples of the IF signal occur exactly on the peaks of the wanted carrier wave. Because the output (video) samples must occur at a rate of 13·3 MHz, the intermediate frequency must be related to this output sample rate. It would be possible to satisfy this condition by making the IF any integral multiple n of 13·3 MHz. The detection process would then consist of selection of every nth IF sample and of feeding it to the video-output terminal.

Although in principle this would be possible, there are certain practical difficulties. The main problem is that in order to be able to define the IF signal there must be a minimum of two samples for each period of the highest frequency component. For the VSB system, and assuming the vision carrier frequency higher than that for sound, the highest frequency is at least 1·25 MHz higher than the vision carrier. In practice, this means that the sample rate must be at least three

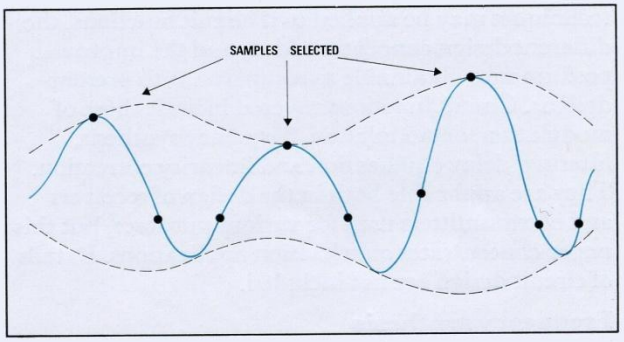


Fig.47. One possible digital synchronous detection process would involve sampling the IF signal at three times the output sample rate and selecting every third sample to feed to the output. The samples of the IF signal have to occur exactly on the peaks of the wanted carrier wave. Since, however, the output sample rate must be 13·3 MHz, this makes the required sampling rate 39·9 MHz which is too high for present devices.

times the vision carrier frequency, i.e. assuming an IF of 13·3 MHz, the minimum sample rate becomes 39·9 MHz and the detection process consists of selecting every third sample.

This is illustrated in Fig.47.
Presently available components are not suitable for operation at these speeds and an alternative approach is necessary. One such alternative is to choose the vision carrier at one-half of the detected output sampling rate. Thus, the vision carrier frequency becomes 6·65 MHz and the samples selected for the detected output are taken alternatively from the positive and negative peaks of the IF signal. A consequence of this arrangement is that the detection process requires alternate samples to be sign reversed. The process is analogous to full wave detection. For the reason given earlier, it is necessary in the IF part of the receiver to employ a sampling rate of at least three times the vision carrier frequency. or 19·95 MHz. Such an arrangement would be possible but, because samples would not occur on both positive and negative peaks, the arrangement would not permit the use of the detection process given above. The preferred arrangement is to use a sample rate four times the vision carrier frquency, or 26·6 MHz. The detection process becomes that of using samples 1 directly, sign reversing and using samples 3, ignoring samples 2 and 4. This is shown diagrammatically in Fig.48.

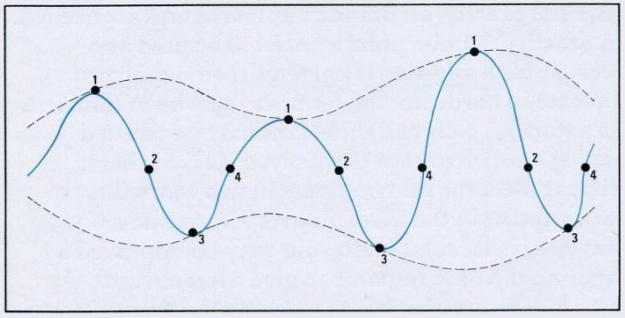


Fig.48. A preferred detection process uses a vision carrier at one-half of the detected output sampling rate. The sample rate is four times the vision carrier frequency (i.e. $4 \times 6{\cdot}65$ MHz) and the detection process then involves using samples 1 direct, sign-reversing and using samples 3 and ignoring samples 2 and 4; the samples used must be located at the peaks of the wanted in-phase component.

It has been said that the samples must be located accurately at the peaks of the inphase component. The criteria are the same as for any synchronous detection process, and in terms of television reception, the accuracy needed is within a degree or so. The way in which this would be achieved is through control of the receiver local oscillator in a 'phase locked loop' as in existing receiver designs. The difference between the output samples 2 and 4 is a measure of phase error, so that after appropriate low pass filtering the difference signal may be used to control local oscillator phase 4. The realization of an all digital phase locked loop has been described in the literature.[5]

Receiver VSB filter

There are applications for digital filters in the IF circuits of both receivers and transmitters. Generally, the requirements of receiver filters are the more stringent and they directly determine the waveform performance; for this reason, receiver filter design is considered in more detail.

Up to the present, designs for vestigial sideband filters have been based upon classical network forms which provide a good amplitude response but at the expense of rather poor phase response. This requires that some provision is made for group delay equalization.

In the previous section it was shown that the synchronous detection process could be performed using a vision carrier frequency of 6·65 MHz and an IF sample rate of 26·6 MHz. Thus, in the IF circuits, all frequency components will be defined up to half the sampling rate, or 13·3 MHz.

For the purpose of this paper, the IF filter will be considered in low-pass form with the 6 dB point at 6·65 MHz. For the reception of UHF (System I) signals this implies that the local oscillator is 0·6 MHz above the wanted sound carrier. The transposition of the wanted and adjacent channel carriers into the IF band is then as shown in Fig.49. Analysis shows that it makes no practical difference whether the IF filter is designed with the vision carrier, which is 6·65 MHz, high or low with respect to the main passband: limitations due to spurious adjacent channel responses are identical.

The wanted carriers in Fig.49 are shown with suffix O and the upper and lower adjacent channel carriers with suffices + and — respectively. The upper adjacent channel carriers are transposed as image responses into the passband. Where an upper adjacent channel signal may be present, some means must be provided for its rejection. Although it could be rejected by use of signal frequency filters, it may be preferable to use a double superheterodyne in which

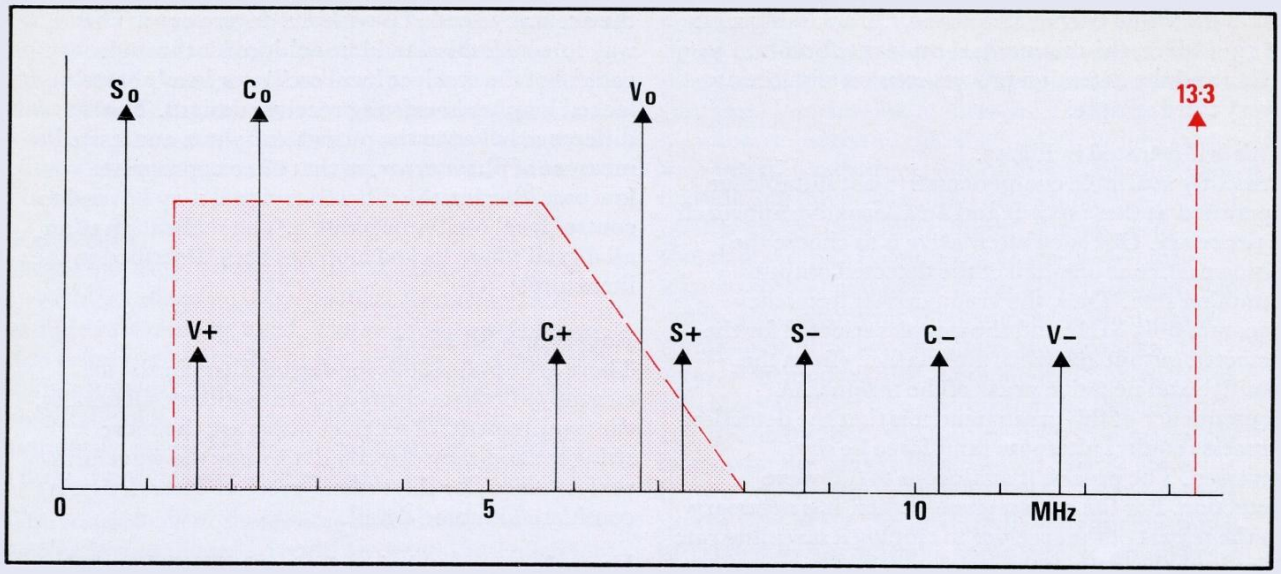


Fig.49. The wanted carriers S_o, C_o, and V_o are shown together with carriers of upper and lower adjacent channels, suffixed + and — respectively. The broken line represents the rf response of an ideal receiver.

the first IF serves the purpose of providing image channel rejection.

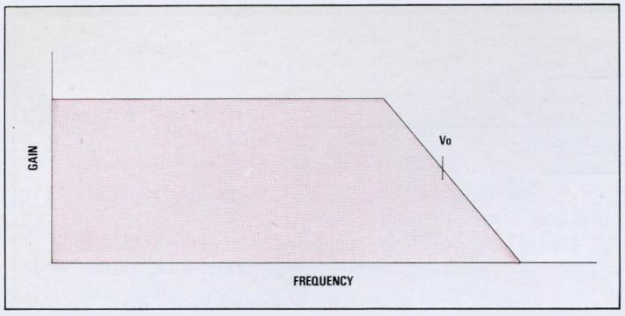
Basically, the design of digital filters falls into two categories, recursive and non-recursive. The details are adequately covered in the literature (references 6, 7, 8, 9) and are merely outlined here.

Recursive filters are referred to more widely; they are more economical when sharp changes in response are needed and they allow the designer to make use of classical designs (Butterworth, Chebychev, etc.). It was mentioned earlier, however, that such designs are in many cases not ideal for vestigial sideband filter applications because of the large inherent phase non-linearity occurring at the flanks of the response.

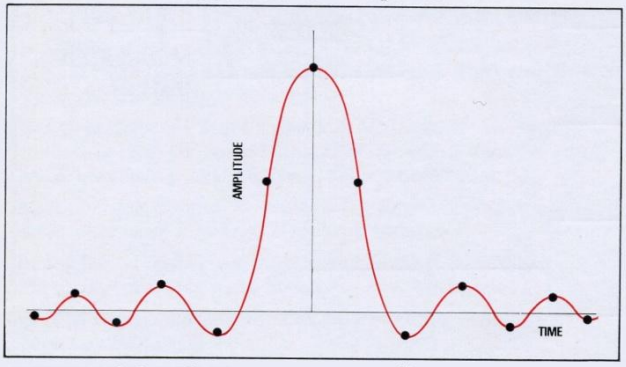
Non-recursive filters include the class referred to as transversal filters. In order to realize a given frequency response, the impulse response corresponding to the specified gain and phase function is calculated and the circuit designed so as to reproduce the same impulse response. For analogue circuits, the hardware would consist of a tapped delay line, various coefficient potentiometers and summing amplifiers. The digital equivalent consists of shift registers, coefficient multipliers and adders. The general arrangement is shown in Fig.50. Any changes in time response which are mirror symmetrical about zero cause only changes in gain with frequency, whereas changes in time response which are skew symmetrical about zero cause only changes in group delay with frequency. It is possible, therefore, independently to vary the gain and delay characteristics of the filter in a manner which is not possible with the more familiar designs.

A problem which arises with this design approach is that in order to realize the required frequency response exactly, an infinite number of taps are needed. In practice, a finite number need to be used and because each additional tap requires a significant increase in hardware the number must be minimized. As a starting point, all those taps may be omitted having coefficients less than, say, 2%. Even here, truncation of the time response in this way will cause ripples in the frequency response and results may not be acceptable. Results may be improved by tapering the time response to give a less abrupt cut-off. The approach is to multiply the time response in Fig.50b by a suitable window function. In the frequency domain, this becomes a convolution and results in a smoother frequency response.[10,11]

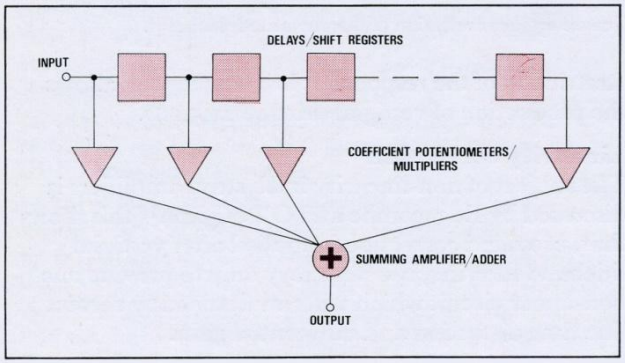
If the passband is truncated to 15 taps, a passband ripple of about 4% is obtained. By reducing the amplitude of the contributions from those taps away from the centre, the ripple may be reduced to nearer 1%. In practice, some of the taps may be arranged to have the coefficient zero and thus reduce the number of multipliers needed.



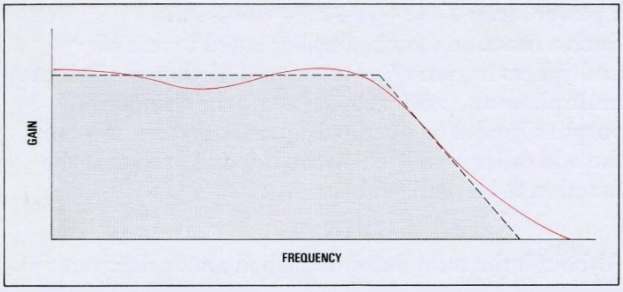
a Ideal receiver IF response.



b Impulse response corresponding to 50a.



c Realization of filter.



d Effect on response of finite number of taps.

Fig.50. Non-recursive filters are preferred for vestigial sideband filter aplications. The design of such a filter for digital circuits would involve the use of shift registers, coefficient multipliers and adders, replacing their analogue equivalents of a tapped delay line, various coefficient potentiometers and summing amplifiers.

Transmitters

In the longer term, video signals may be distributed to transmitting stations over digital links. There would be advantage in directly converting these digital video signals into amplitude modulated rf signals also coded into digital form.

If a digital modulator is employed, the resulting IF may be digitally filtered and applied to digital linearity pre-correction circuits. As for receiver IF circuits, the transmitter IF filter may be designed to provide the necessary vestigial sideband characteristic.

Modulator

The input video is assumed to be in a form of eight-bit words at a rate of 13·3 MHz. Following from the discussion in the receiver section, the modulation process consists basically of sign reversing alternate samples. This would give a vision carrier at 6·65 MHz but with the waveform defined only up to carrier frequency so that upper and lower sidebands would not be distinguished. The response can be defined to 13·3 MHz if additional samples are interleaved. In order to produce a perfect double sideband wave, these extra samples must all take the value zero and the modulation process is seen to be the reverse of that for synchronous demodulation. It is of interest to note that although the resulting IF has a carrier frequency of 6·65 MHz and a data rate of 26·6 MHz, the A:D converter used to digitize the video signal needs to operate only up to a rate of 13·3 MHz. By artificially adding intermediate samples all of value zero, it is ensured that the quadrature component and hence phase modulation of the wave is zero. The process may be described as synchronous modulation.

The digitally coded IF signal may be converted into analogue form by use of a D:A converter. Unless the D:A converter output is in the form of pulses which are of short duration compared with the interval between samples, then some small variation in gain with frequency occurs. In practice, it is convenient to use relatively broad output pulses and to compensate for the frequency response error in the vestigial sideband filter.

The advantages in the use of this type of modulator would be the avoidance of black level clamps, the possibility of achieving extremely good linearity, and the elimination of incidental phase modulation which can cause a buzz from receivers employing intercarrier sound reception.

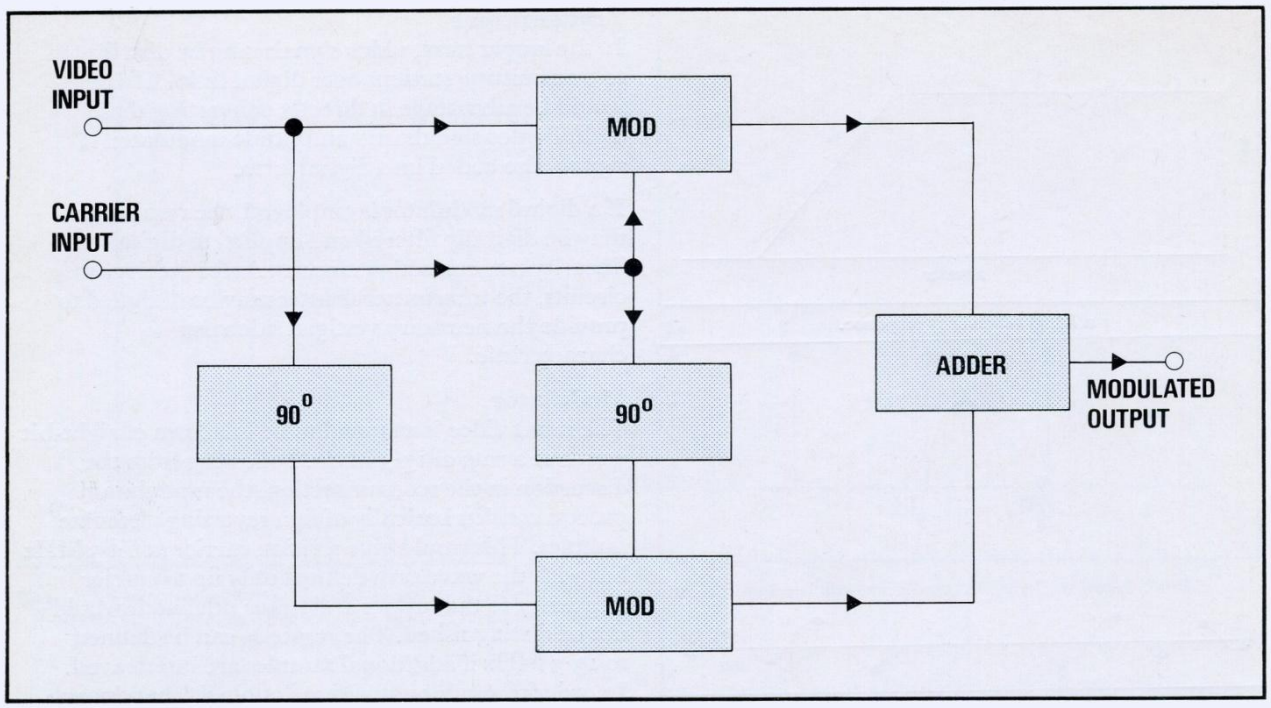


Fig.51. The diagram shows an arrangement for vestigial sideband signal generation. Digital techniques are particularly favourable here since an accurate balance is required between the two channels to cause total cancellation of the unwanted sideband.

VSB Filter

The characteristic needed is given in the literature.[12] Practical design problems are similar to those encountered in receiver IF circuits. In general, the high power outputs from vision and sound klystrons need to be added in a frequency selective combining unit filter.[13] This filter causes a rise in group delay at the edge of the sideband nearest the sound carrier frequency. The delay may be compensated for in the design of the digital vestigial sideband filter.

An alternative method of generating a vestigial sideband signal is to use a quadrature modulator. The principle, using analogue circuits, was suggested by Gouriet and Newell,[14] it is based on the generation of two double sideband signals which when added together form a vestigial sideband signal. The block diagram is shown in Fig.51. An arrangement such as this is particularly suitable for realization in digital form because it requires an accurate balance between the two channels in order to achieve cancellation of the unwanted sideband. If the 90° network in the video path shown in Fig.51 has a frequency response extending from low frequencies over the whole video band, then a single sideband signal will result. Restriction of the response at low frequencies allows the production of vestigial sideband signals.

Linearity correction

The subject of non-linearity in klystron amplifiers is discussed by Edgecombe and O'Loughlin[15] this shows that, provided correction is applied after vestigial sideband filtering, it is necessary only to provide one non-linear circuit which will simultaneously correct line time distortion and differential gain.

Any desired non-linear function may be expressed as a power series $Y=a+bx+cx^2+dx^3+\ldots$
Such a function may be implemented by use of multipliers to give x^2, x^3 terms and further coefficient multipliers and adders to generate the composite output signal. For a radio frequency system, it is only the odd order terms which are important so that the function to be realized becomes:

$$Y=x+dx^3+$$

Although the modulator described above does not introduce spurious phase errors, present-day klystrons do cause some incidental phase modulation amounting to about 10°. This could be compensated in the modulator by interleaving samples which are derived from an appropriate non-linear function of the video

signal, instead of the samples of value zero as proposed above.

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Oracle — Broadcasting the Written Word

Engineers of the IBA have recently developed and demonstrated an experimental data system, Oracle, capable of providing a continuous public information service on conventional television transmitting networks. With this system the public could receive up to 50 different 'pages' of information 'written' on their television screens, each page containing up to 880 characters, or roughly 120 words. These messages can be displayed or superimposed on the screen of a domestic television receiver without in any way affecting the reception of normal television programmes.

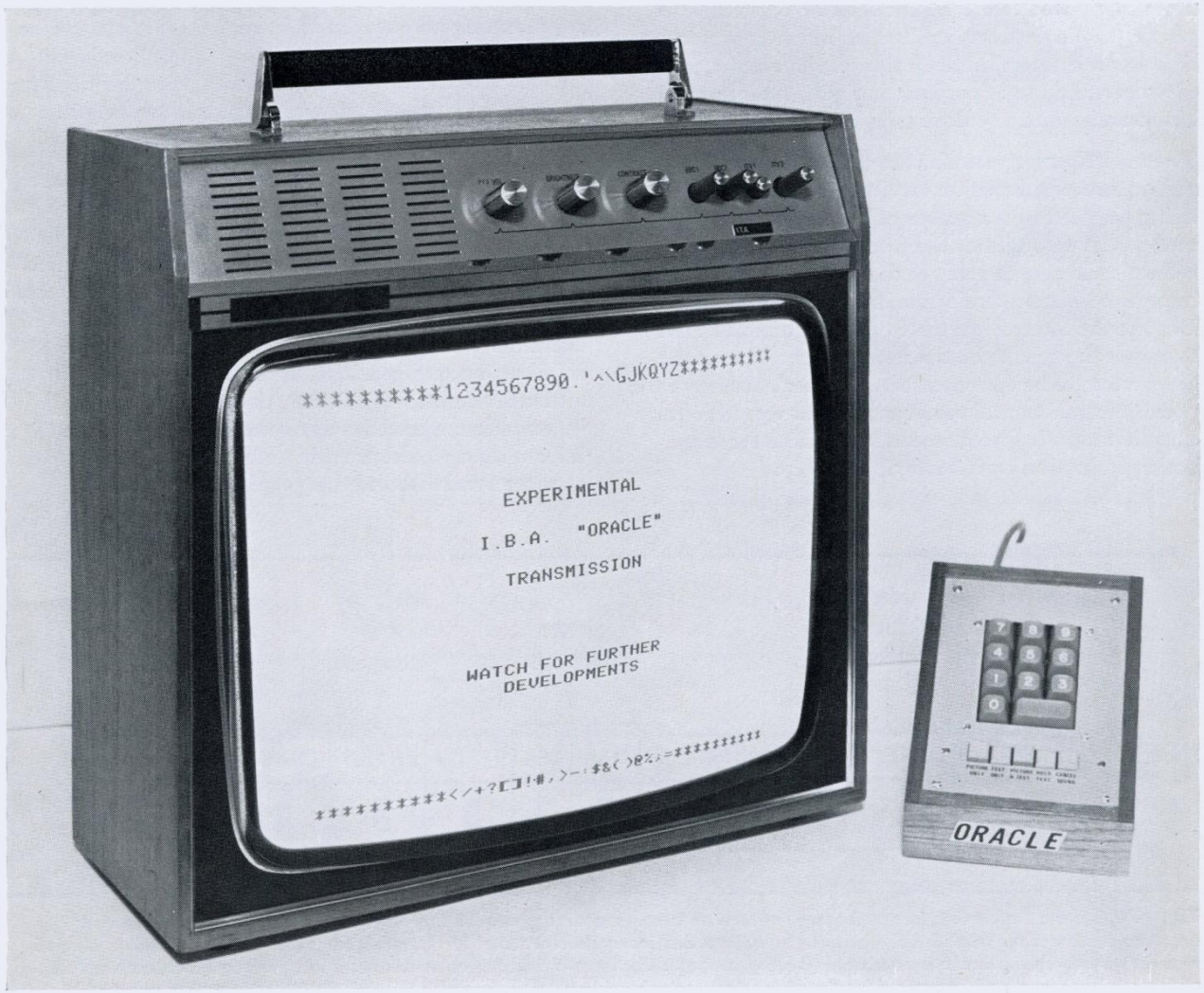

Fig.52. The Oracle 'test card' displayed on a television receiver with *(right)* the Oracle push-button control unit.

The idea of data broadcasting services is not new, and in various forms they have been proposed many times before; the IBA's Oracle system, however, is believed to be not only more flexible and to offer more facilities than the earlier proposals, but also has already reached a stage of development where its operation can be demonstrated on experimental transmitting and receiving terminals. Experimental Oracle transmissions are being made on the IBA's London television stations to test the experimental receiving unit which has been assembled at the IBA's London headquarters. The system draws heavily on the techniques developed for the IBA's SLICE system which has been fully field-tested as a means of identifying picture sources.

It is anticipated that if a firm decision was made to start a public data service, British industry would be able to produce suitable Oracle adaptor units, which viewers could use in conjunction with their normal black-and-white or colour television receivers.

The underlying reason for the current interest in public data transmission services – similar work is being pursued by a number of broadcasting authorities throughout the world – is the dramatic reduction in recent years of the cost of complex digital integrated-circuit devices, suitable for data storage. Despite the intense interest in such systems, the IBA system is thought to be the most advanced, and the first system to be demonstrated 'off air', although the present experimental receiver adaptor would require simplification before it would be suitable for large scale production by industry.

What Oracle offers

The adoption of Oracle would mean that a viewer would require an adaptor unit which he would use in conjunction with his normal television set and a small pushbutton keyboard control unit. By means of the pushbutton control he could at any time cause to be displayed on his screen any one of 50 'pages' of information. These messages would be displayed in the form of clear electronic letters or numerals or graphical symbols on his screen, either briefly replacing his television picture or even superimposed on top of it. Any type of written information could be sent, one page at a time, with the individual pages updated at regular intervals. Since it takes 1·8 seconds maximum for the transmission of one page of this material, it is possible for the 50 pages – each perhaps representing an entirely different information service – to be updated or rewritten in a period of less than two minutes. The viewer would also have the facility to 'hold' indefinitely any page of this information.

The type of information services which could be provided by such a public broadcast data service are almost unlimited, and the system has many other potential applications for home or business use. The type of information services which could be provided in this way includes continuous accurate time checks, weather forecasts, news, traffic, and local news, stock exchange prices, television and radio programme information, recipes, local and national announcements, exhibitions, theatres, shopping information, and advertising messages. One page of information would provide a summary of the services available and the 'page number' which

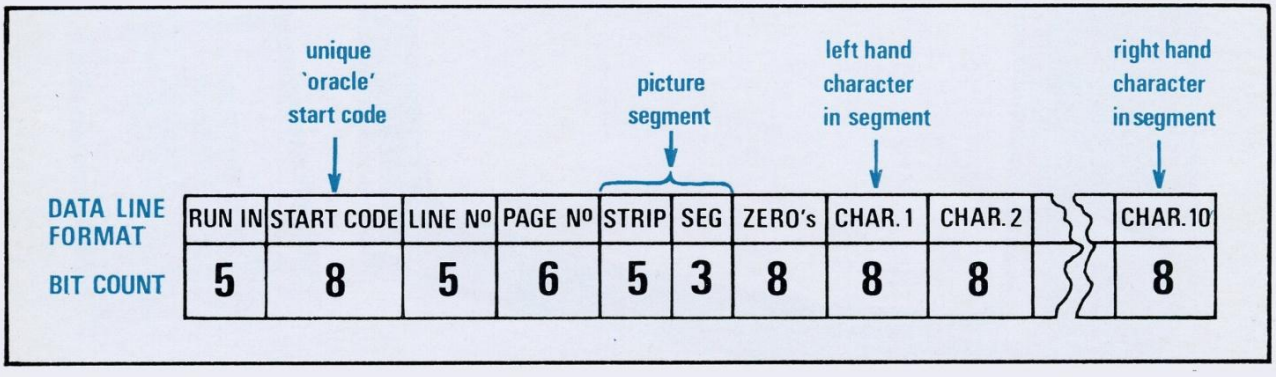

Fig. 53. This is the Oracle data format for one 'segment' representing one quarter of a line of written information. Each segment occupies one line of the television signal in the unused vertical intervals. Normally the Oracle signal would be transmitted on Line 16 and the corresponding line in the odd field (that is Line 329). The form of modulation used is known as 'complemented element' in which a '1' is represented by a transition from picture white to black and '0' by the reverse transition. This form of modulation is rugged and unlikely to suffer errors during transmission and has been well tested.

would be used by the viewer to 'call up' the display on his screen. Other possibilities include the use of the equipment as a home data terminal, the provision of caption material to accompany television programmes for the deaf viewer or for those who do not understand the language of the programme.

The display letters would be formed from a 'matrix' using techniques already widely used in computer visual display units and in electronic character generators. Oracle however has sufficient flexibility to contemplate further possibilities such as the use of individually coloured letters or graphical symbols. The possibility also exists of providing 'electronic newspapers' transmitted at night and recorded automatically.

Two 64 μs 'line periods' repeating at the rate of 25 per second, are more than sufficient to allow the amount of data envisaged in an Oracle service to be transmitted. During each brief Oracle transmission period – that is 64 μs 50 times a second – one 'segment' of display information, representing up to 10 characters, is transmitted together with its 'address code'. This address indicates to the receiving unit the exact position on the screen and for which page the information relates. This signal is in the form of a 'run-in code' (five binary digits or bits); a 'start code' (eight bits); a 'line number' (five bits); the field or 'page' number (six bits); and the address (eight bits). The data format is shown in Fig.53. A 'message' of up to ten letters can be transmitted on each line. Each line thus provides a data communications capacity equivalent to a telephone line.

At the sending end, the text of a page is prepared in advance on a computer terminal unit. The various pages are entered and held in the memory of a small general-purpose computer which allows the information to be inserted into the television signal in the correct form at the appropriate time. When the page has been completed it is transmitted in approximately 1·5 seconds, so that the total time for transmitting all 50 pages – in effect a small 'book' of written information – does not exceed about 1 min. In the present experimental system the text is restricted to a standard type-face of some 60 characters, but the code used will allow for an extension of this; the text can incorporate non-typographical signs to allow the transmission of drawings or even free-hand writing. As indicated, the text is transmitted in segments of 10 characters with each character represented by an eight-bit code.

At the receiving end, the domestic television set requires adaption for Oracle either by means of an independent add-on unit or, more cheaply, by an internal modification. The system now undergoing test allows for 50 pages of text, each consisting of 22 lines of 40 characters, and the experimental

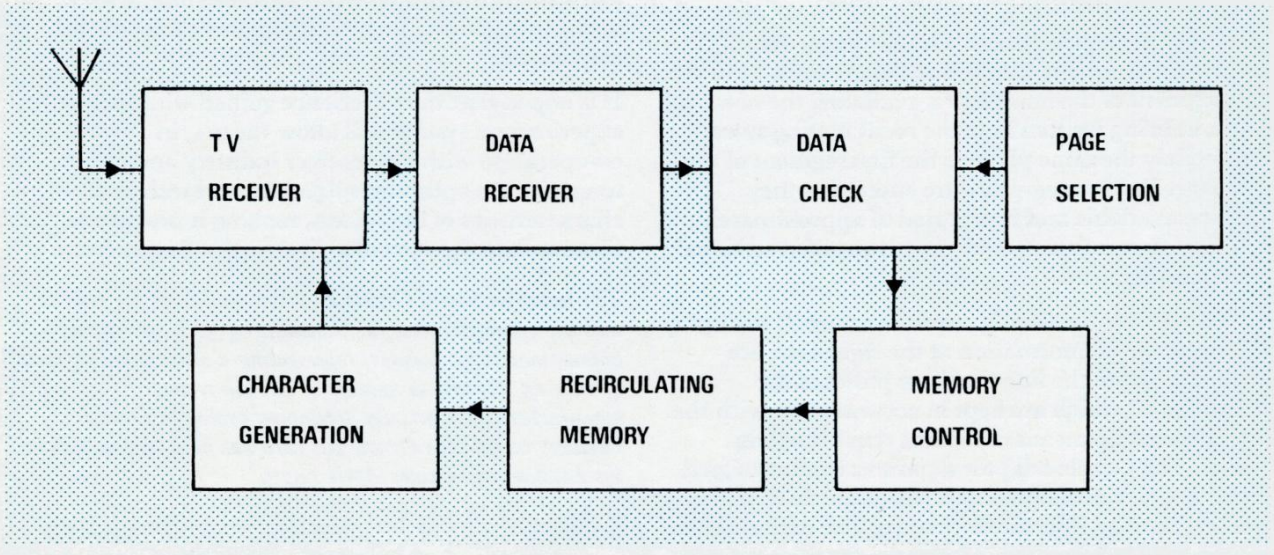

Fig.54. A block diagram showing the main elements of an Oracle receiving system. The Oracle circuits could be provided either by means of an independent add-on unit used in conjunction with an existing receiver or, rather more cheaply, by modification of the design of a receiver to provide built-in Oracle circuits. British industry has already shown keen interest in the development of a public data system based on the Oracle principles.

receiver adaptor enables the user to select any page for display. The equipment at the receiver, Fig.54, is in principle simple. The data is extracted from the television; checked to see whether it is Oracle data; if it is, the page number is read and when this coincides with the number selected by the viewer, data is fed into an intermediate store capable of storing the ten characters transmitted in the single field interval. Subsequently, at the appropriate moment, the data is fed out of this store into the main recirculating store capable of storing a complete 'page' of Oracle information, that is to say 880 characters in 88 segments, or 5,280 bits. A third store completes the sequence, holding a complete line of 40 characters, that is four segments of information, and is up-dated by the recirculating store. The signal from the third store is presented to the character generator one character at a time. Each character is based on the 7 by 5 dot-matrix. On the television picture the characters are built up line by line by demodulating the scanning beam in the appropriate way, i.e. the scanning beam is modulated in rapid succession by the first row of squares for each of the letters in a line of text, followed by the second row and so on until the complete text has been displayed. To achieve this the information from the third store is presented character by character in rapid succession seven times. The line of text is followed by a space four television lines wide. Before these are scanned the third store is reloaded from the main recirculating store.

On switching to a different 'Oracle' page, the recirculating store is emptied and then waits until the first segment of the new page is available, the new segment being written in to the recirculating store in precisely the same place as the first segment of the old page. Further segments are entered as they become available and in a period of approximately 1·5 seconds a complete new page is transferred to the recirculating store.

At the receiver the timing sequences needed to display the segments of information at the right time are controlled from the line timebase pulses of the television set which are kept in accurate step with the transmission by means of the line synchronizing pulses. The Oracle adaptor separates the data signal from the television signal and passes the data, in 64 μs packets, into an intermediate store. The address code is then used to insert the information at the precisely right moment into the main store where the complete 'page' of information is held ready for display. Each character is based on a matrix of 7×5 dots. The main store has to be capable of holding 5,280 bits of information, and in practice this store consists of a recirculating shift register in integrated circuit form.

At the studios, the various Oracle pages would be kept updated by an editorial team working within a communications complex and using visual display units and keyboards in conjunction with a central computer which would be needed to collate the information so that it can be inserted into the television waveform at the appropriate moments and distributed along with the normal television signals to the transmitting stations. The first line of each page would carry an identification, date and time so that every viewer, no matter which of the Oracle services he was watching, would have the equivalent of a highly accurate digital clock always available. For example the first line might read: ORACLE 33 PAGE 22 21 APR 17: 21: 07. This would identify the page being transmitted as 33, the page of information displayed (22), the date (21 April) and the time 17 hours, 21 minutes, 7 seconds.

The experimental receiving unit developed and demonstrated by the IBA is significantly larger and more complex than would be necessary for a domestic Oracle adaptor. Furthermore, advances in large scale integration of the memory devices would drastically cut down the number of devices required in the main store. It is possible that this might in future consist of just a single integrated circuit for the store, with a second chip containing virtually the entire control electronics.

It is hoped that the experience gained with this experimental system will allow the IBA, in co-operation with the receiver industry and others, to specify the optimum subjective and technical characteristics of the system, making it possible to contemplate the start of a pilot public data service.

The latest version of Oracle uses two data lines per field so that the maximum time for transmitting 50 pages is only approximately 30 seconds, representing a mean 'waiting time' of only 15 seconds. A number of British receiver manufacturers are actively developing prototype Oracle receiving units. The Oracle test card has been transmitted in the London region since April 1973.

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